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Docket No.: M4065.0985/P985
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Chandra Mouli

Application No.: 10/680,158

Confirmation No.: 5806

Filed: October 8, 2003

Art Unit: 2814

For: 1T/0C RAM CELL WITH A WRAPPED-AROUND GATE DEVICE STRUCTURE

Examiner: H. Weiss

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed in furtherance of the Notice of Appeal, filed in this case on September 25, 2006.

The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument
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Appendix A	Claims

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Appendix B	Evidence
Appendix C	Related Proceedings

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

MICRON TECHNOLOGY, INC., a corporation organized under and pursuant to the laws of the State of Delaware, and the assignee of this application.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 67 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 0
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 1-67
4. Claims allowed: 0
5. Claims rejected: 1-67

C. Claims On Appeal

The claims on appeal are claims 1-67

IV. STATUS OF AMENDMENTS

Appellant filed a response to the Final Rejection on August 18, 2006, which did not contain any proposed claim amendments. There have been no claim amendments since the Final Rejection was mailed and all previous amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a *storage* transistor having a wrapped-around gate structure for use in a memory cell, and particularly for use in a one transistor capacitor-less (1T/0C) DRAM cell. The storage transistor is configured to employ any of the following means to generate charge to be stored in the storage transistor: a) impact ionization; b) band-to-band tunneling; and c) channel-initiated secondary hot electrons (CHISEL). A combination of these three methods can be used to increase carrier generation efficiency. Carriers, *e.g.*, holes, generated by these methods are stored in the body of the storage transistor during a write operation. *See* Appellant's specification at p. 5-6.

According to an exemplary embodiment of the invention, the storage transistor is a fin-type field effect transistor (FinFET) provided for a 1T/0C DRAM cell. As is known in the art, a FinFET is a multiple-gate field effect transistor that is typically a fully depleted (FD) silicon-on-insulator (SOI) device used in advanced logic technologies. *Id.* at p. 6-7. FD-SOI FinFET's are typically designed to *eliminate* what is known as a floating body effect (FBE). *Id.* at p. 7.

A floating body effect causes fluctuation in the threshold voltage for the device caused by charge build up in a body of the FinFET; this effect is detrimental to the operation of the FinFET. *Id.* Because the presence of a floating body effect is detrimental to its operation, an FD-SOI device (including an FD-SOI FinFET) is *not* considered a suitable device for storing charge as is needed in a DRAM cell. The inventors have determined that, contrary to conventional wisdom, a FinFET *can* be used as a storage device. Therefore, embodiments of the invention provide a partially depleted (PD) memory storage transistor, including, but not limited to a FinFET[1], with an increased floating body effect over a FD-SOI device. *Id.* Advantages of the claimed invention include increased charge storage due to an increased active area of the body and gate portions.

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[1] Although the preferred embodiments of the present application include a FinFET structure, Appellant notes that none of the "gate" or "gate structure" limitations in independent claims 1, 23, 28, 30, 32 or 47 are exclusively

Independent claims 1, 23, 28, 30, 32 and 47 are pending. Pursuant to 37 C.F.R. §41.37(c), Appellants provide the following summary of the claimed subject matter on appeal.

Independent claim 1 recites a memory device, an example of which is described in the specification at pages 7-9, ¶ 40-47, pages 5-16, ¶ 71-75 and shown in Fig. 2, 3, 4 and 9A[2]. Fig. 3, reproduced below, is a diagram of an exemplary embodiment of the memory device 200; Fig. 4, reproduced below, is a cross section of the memory device 200 of Fig. 3 along the X direction; and Fig. 9A, reproduced below, is an alternate embodiment of the memory device 200 of Fig. 3 corresponding to a cross section of the memory device 200 along the Y direction. The memory device 200 of claim 1 comprises: a storage transistor 201 at a surface of a substrate 215, the storage transistor 201comprising: a body portion 217 between first and second source/drain regions 230, 235, wherein the first and second source/drain regions 230, 235 are regions of a first conductivity type, each of the first and second source/drain regions 230, 235. As shown by Fig. 9A and as described in Appellants' specification at page 15, ¶ 71, embodiments of these first and second source/drain regions 230, 235[3] may including a plurality of layers 904-1 – 904-n (Fig. 9A) capable of generating carriers through impact ionization, and a gate structure 220, wherein the gate structure 220 wraps at least partially around the body portion 217; a bit line 296 (Fig. 2) connected to the first source/drain region 230; and a word line 298 (Fig. 2) connected to the gate structure 220.

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limited to FinFETs. Similarly, although the Final Office Action relies on the FinFET disclosed by the Pham reference as disclosing the relevant "gate" or "gate structure" limitations in independent claims, the language of the individual claims are not so limited unless they explicitly recite a FinFET.

[2] Fig. 3 and 4 are different views of the same embodiment with Fig. 4 being a cross section of Fig. 3. The memory device 200 of Fig. 9A is a variation of the memory device 200 of Fig. 3-4. *See* Appellants' Specification at p. 10, ¶ 50 and p. 13, ¶ 63.

[3] Due to a typographical error, Fig. 9A uses the reference numbers 930 and 935 for source/drain regions 230 and 235. In the context of the written description of this figure, which assigns the reference numbers 230 and 235 to the source/drain regions of Figs. 3, 4 and 9A, it is apparent that these embodiments show different aspects of the same underlying structure.

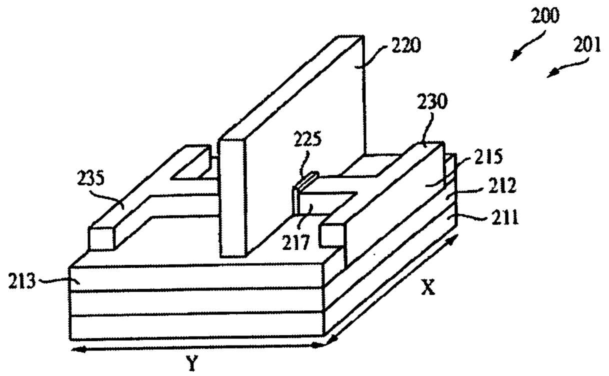


FIG. 3

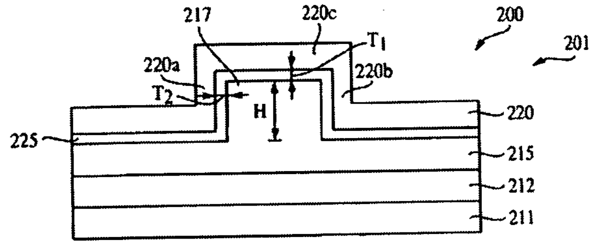


FIG. 4

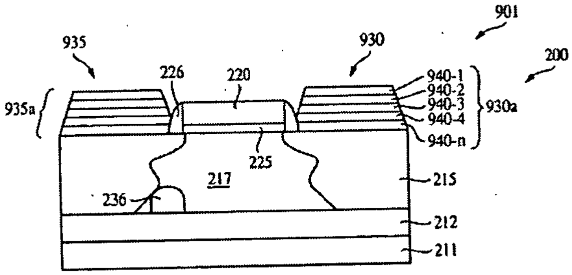


FIG. 9A

Independent claim 23 recites a dynamic random access memory (DRAM) cell, an example of which is described in the specification at pages 7-9, ¶ 40-47, pages 5-16, ¶ 71-75 and shown in Fig. 2, 3, 4, 5 and 9A. Fig. 5, reproduced below, is a cross section of the memory device 200 of Fig. 3 along the X direction. The DRAM cell 200 of claim 23 comprises: a storage transistor 201 at a surface of a silicon-on-insulator (SOI) substrate 215 According to claim 23, the storage transistor 201 comprises: a body portion 217 between first and second source/drain regions 230, 235, the body portion 217 containing a heavily doped region 236 (Fig. 5, *see also* Fig. 9A) of a first conductivity type adjacent to the second source/drain region 235 and separated from the first source/drain region 230, the first and second source/drain regions 230, 235 being regions of a second conductivity type, and a gate structure 220, the gate structure 220 wrapping at least partially around the body portion 217 in at least two spatial planes (the vertical and horizontal surfaces of body portion 217; *see* Fig. 3 and 4); a bit line 296 (Fig. 2) connected to the first source/drain region 230; and a word line 298 (Fig. 2) connected to the gate structure 220.

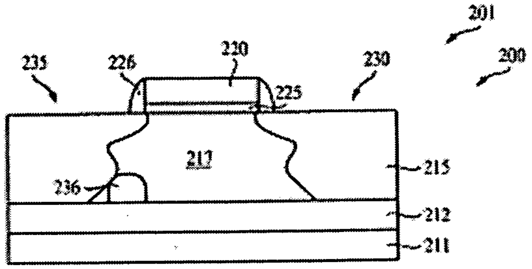


FIG. 5

Independent claim 28 recites a memory array, an example of which is described in the specification at pages 7-9, ¶ 40-47, pages 5-16, ¶ 71-75, page 17, ¶ 81 and shown above in Fig. 3, 4, 5, 9A and 11. The memory array 299 (Fig. 11) of claim 28 comprises: a plurality of memory cells 200, each memory cell 200 comprising a storage transistor 201 at a surface of a silicon-on-insulator (SOI) substrate 215. The claim 28 storage transistor 201 comprises: a body portion 217 between first and second source/drain regions 230, 235, the body portion 217 containing a heavily doped region 236 (Fig. 5, *see also* Fig. 9A) of a first conductivity type adjacent to the second source/drain region 235 and separated from the first source/drain region 230, the first and second source/drain regions 230, 235 being regions of a second conductivity type, and a plurality of gates 220a, 220b at least partially surrounding the body portion 217 (*see* Fig. 3 and 4); a bit line 296 (Fig. 2) connected to the first source/drain region 230; and a word line 298 (Fig. 2) connected to at least one gate 220a, 220b.

Independent claim 30 recites a semiconductor chip, an example of which is described in the specification at 7-9, ¶ 40-47, pages 5-16, ¶ 71-75, page 17, ¶ 81 and shown above in Fig. 3, 4, 5, 9A and 11. The semiconductor chip 1100 of claim 30 comprises: a plurality of dynamic random access memory (DRAM) cells 299, at least one DRAM cell 200 comprising a partially depleted storage transistor 201 at a surface of a silicon-on-insulator (SOI) substrate 215. The claim 30 storage transistor 201 comprises: a body portion 217 between first and second source/drain regions 230, 235, the body portion 217 comprising at least one fin-shaped structure (*see* Fig. 3 generally) and a region 236 (Fig. 5, *see also* Fig. 9A) of a first conductivity type adjacent to the second source/drain region 235, the first and second source/drain regions 230, 235 being regions of a second conductivity type and each of the first and second source/drain regions 230, 235 including a plurality of layers 901-1 – 901-n capable of generating carriers through impact ionization, and a gate structure 220, the gate structure 220 wrapping at least partially around each fin-shaped structure [of body portion 217]; a bit line 296 connected to the first source/drain region 230; and a word line 298 connected to the gate structure 220.

Independent claim 32 recites a processor system, an example of which is described in the specification at 7-9, ¶ 40-47, pages 5-16, ¶ 71-75, page 18, ¶ 83 and shown in Fig. 3, 4, 5, 9A and 12. The processor system 1200 of claim 32 comprises: a processor 1202 coupled to a memory device 1100, the memory device 1100 comprising a plurality of memory cells 299, each memory cell 200 comprising a storage transistor 201 at a surface of a substrate 215. The claim 32 storage transistor 201 comprises: a body portion 217 between first and second source/drain regions 230, 235, the first and second source/drain regions 230, 235 being regions of a first conductivity type and each of the first and second source/drain regions 230, 235 including a plurality of layers 904-1 – 904-n capable of generating carriers through impact ionization, and a gate structure 220, the gate structure 220 wrapping at least partially around the body portion 217; a bit line 296 connected to the first source/drain region 230; and a word line 298 connected to the gate structure 220.

Independent claim 47 recites a transistor device, an example of which is described in the specification at pages 7-9, ¶ 40-47, pages 5-16, ¶ 71-75 and shown in Fig. 3, 4 and 9A. The transistor device 200 comprises: a first source/drain region 230 of a first conductivity type; a second source/drain region 235 of a first conductivity type; a body portion 217 for storing charge, the body portion 217 protruding from a surface of a substrate 215, the body portion 217 being located between the first and second source/drain regions 230, 235, the body portion 217 including a doped region 236 of a second conductivity type adjacent to the second source/drain region 235 and separated from the first source/drain region 230; and a gate structure 220 wrapping around the body portion 217 in at least two spatial planes.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 and 62-67 under 35 U.S.C. 103(a) as being unpatentable over "Memory Design Using One-Transistor Gain Cell on SOI" by Ohsawa et al. (2002 IEEE International Solid State Circuits Conference) ("Ohsawa") (attached as Exhibit 1 in Appendix B) in view of U.S. Patent No.

6,838,322 to Pham et al. ("Pham") (attached as Exhibit 2 in Appendix B), and further in view of U.S. Patent No. 6,313,486 to Kencke et al. ("Kencke") (attached as Exhibit 3 in Appendix B).

B. The rejection of claims 8 and 35 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 5,448,513 to Hu et al. ("Hu") (attached as Exhibit 4 in Appendix B).

C. The rejection of claims14-16, 38-40 and 59-61 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 6,806,537 to Matsumoto et al. ("Matsumoto") (attached as Exhibit 5 in Appendix B).

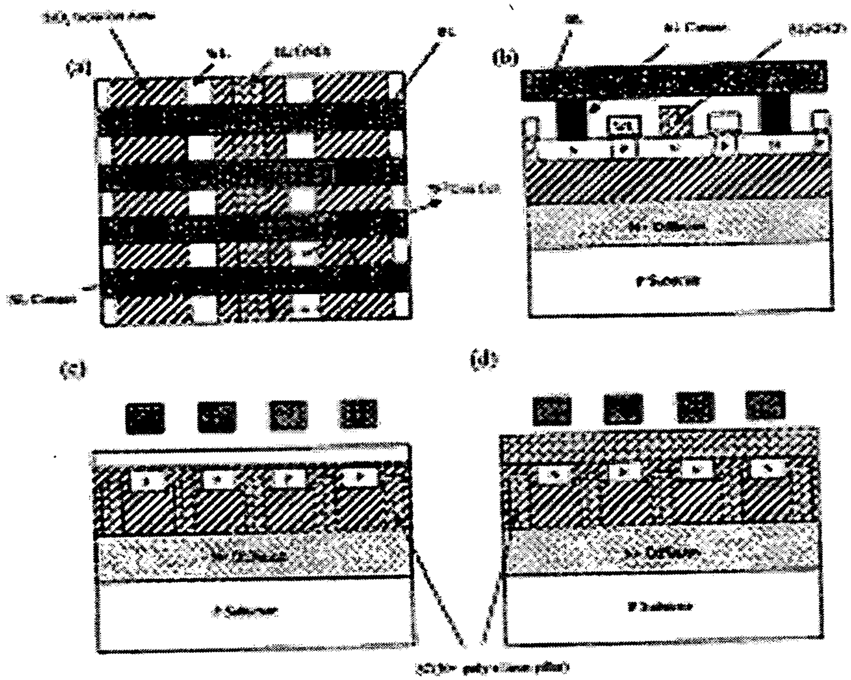
D. The rejection of claims 15 and 58 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 5,307,305 to Takasu (attached as Exhibit 6 in Appendix B).

E. The rejection of claims 15 and 58 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 6,221,724 to Yu et al. ("Yu") (attached as Exhibit 7 in Appendix B).

VII. ARGUMENT

A. CLAIMS 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 AND 62-67 ARE PATENTABLE OVER OHSAWA IN VIEW OF PHAM AND FURTHER IN VIEW OF KENCKE (GROUND OF REJECTION A).

Each of claims 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 and 62-67 recite a storage transistor having a gate structure wrapping at least partially around a body portion (as described above in Section V). As will be shown below, Appellant respectfully submits that, absent improper hindsight, there is no motivation to combine the teachings of Ohsawa and Pham to achieve the claimed invention. Ohsawa discloses a storage transistor, but does not disclose a gate structure which at least partially wraps around a body portion. Figure 9.1.1 of Ohsawa, reproduced below, instead discloses a planar device having smaller active areas, the drawbacks of which are described in Appellants' specification at p. 7.



[illegible]

Pham discloses a FinFET having a gate structure which at least partially wraps around a body portion (see Fig. 1 of Pham, reproduced below), but there is no disclosure, teaching or suggestion to use the FinFET of Pham as a storage transistor to meet the limitations of the claims. In fact, as explained below, Pham explicitly teaches away from using its FinFET as a memory storage transistor. Appellant respectfully submits that this rejection is based improperly on hindsight and should be reversed.

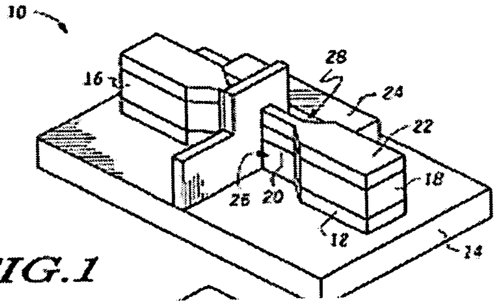


FIG.1

Moreover, Kencke, relied on as teaching source/drain regions consisting of layers of Si_xGe_{1-x} and Si_yGe_{1-y} with different band gaps and capable of generating carriers through impact ionization, also fails to disclose, teach or suggest the use of a transistor having a gate structure wrapping around a body portion (*e.g.*, a FinFET) as a storage transistor, or the use of the layered source/drain regions in the transistor structure of Ohsawa or Pham. Because none of Ohsawa, Pham or Kencke disclose teach or suggest the use of a transistor having a gate structure wrapping around a body portion as a storage transistor having all of the claimed features, and because Pham actually teaches away from a wrap around gate feature, the rejection is improper and should be reversed.

1. Claims 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 and 62-67 all contain limitations relating to a storage transistor having a gate structure which wraps at least partially around a body portion.

Independent claim 1 recites a memory device comprising, *inter alia*, a "*storage transistor* comprising: a body portion between first and second source/drain regions," each "including a plurality of layers capable of generating carriers through impact ionization," and "a gate structure, *wherein the gate structure wraps at least partially around the body portion*." The other independent claims recite similar features.

For example, independent claim 23 recites a "dynamic random access memory (DRAM) cell" comprising, *inter alia*, a "*storage transistor* comprising: a body portion between first and second source/drain regions, the body portion containing a heavily doped region of a first conductivity type adjacent to the second source/drain region and separated from the first source/drain region" and "a gate structure, *the gate structure wrapping at least partially around the body portion* in at least two spatial planes."

Likewise, independent claim 28 recites a "memory array" comprising, *inter alia*, "a plurality of memory cells, each memory cell comprising a *storage transistor*," the storage transistor comprising a "body portion containing a heavily doped region of a first conductivity type adjacent to [a] second source/drain region and separated from [a] first source/drain region," the storage transistor further comprising "a *plurality of gates at least partially surrounding the body portion*."

Similarly, independent claim 30 recites a "semiconductor chip" comprising, *inter alia*, "a plurality of dynamic random access memory (DRAM) cells, at least one DRAM cell comprising a partially depleted *storage transistor*" having "first and second source/drain regions including a plurality of layers capable of generating carriers through impact ionization" and "a gate structure, the *gate structure wrapping at least partially around each fin-shaped structure*."

In addition, independent claim 32 recites a processor system comprising, *inter alia*, a "*storage transistor* comprising: a body portion between first and second source/drain regions," each "including a plurality of layers capable of generating carriers through impact ionization," and "a gate structure, *wherein the gate structure wraps at least partially around the body portion*."

Finally, independent claim 47 recites a "transistor device" comprising, *inter alia*, "*a body portion for storing charge*, . . . the body portion including a doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region" and "*a gate structure wrapping around the body portion* in at least two spatial planes."

2. Ohsawa is relied on for the disclosure of a "storage transistor," and Pham is relied on for the disclosure of a "gate structure at least partially wrapping around the body portion", but there is no motivation to combine the two references.

The Final Rejection of May 24, 2006, admits, at p. 2-3, that Ohsawa does not "show the storage transistor as a FinFET with a gate structure wrap[ping] around the body portion in at least two planes and consisting of a plurality of gates." Ohsawa teaches a memory based on a one-transistor gain cell. In order to accomplish Ohsawa's one-transistor gain cell, a *planar* MOSFET with an electrically floating body is used. Ohsawa at p. 1510, Section II. Pham, on the other hand, teaches a fabrication process for forming a FinFET.

Appellant respectfully submits that there is no motivation to combine Pham with Ohsawa for two reasons. First, there is no disclosure, teaching or suggestion in the references themselves to combine these teachings, and the Final Rejection does not rely on any other explicit or implicit evidence of motivation to combine. Second, Pham explicitly teaches away from using the disclosed FinFET as a storage transistor, and therefore cannot serve to create a prima facie case of obviousness.

a. There is no disclosure, teaching or suggestion in Ohsawa or Pham to use the FinFET of Pham as a storage transistor

It is understood by those skilled in the art that FinFETs provide very good gate control in the sub-threshold and linear regions. FinFETs allow use of an undoped channel and can be fully depleted devices. *See* Appellant's Specification at p. 6-7. As mentioned in Pham, when planar devices, such as Ohsawa's MOSFET, are scaled, intense channel doping is needed. However, the channel doping degrades carrier mobility and junction characteristics, which according to Pham is undesirable. Pham at col. 1, lines 25-34. As such, the fabrication processes described by Pham do not include channel doping, which is needed to achieve the floating body effect (described above) necessary for a storage transistor of the claimed invention. Specification at p. 9, Fig. 5; *see also* Fig. 9A.

There is no suggestion in Pham that the disclosed FinFET could be used as a storage transistor. Appellant's claimed storage transistor relies on a substantial floating body effect in its operation (see specification at p. 7); Pham does not discuss how its FinFET may be used as a storage device, or how the FinFET is in any other way suited for use as a storage transistor in a memory cell. The constraints required for a conventional FinFET, as taught by Pham, are very different from the constraints required for constructing the storage device claimed by Appellant. Appellant found that a FinFET (and other transistors having a gate structure which wraps around a body portion)[4] could be used as a storage device by both doping the channel to achieve a floating body effect, and suitably doping source/drain regions (*see, e.g.*, Appellants' specification at p. 9, Fig. 5 and 9A). Absent Appellant's disclosure, however, the Final Rejection has not shown any other motivation anywhere in the prior art at the time the invention was made where a FinFET or other similar transistor having a gate structure which at least partially wraps around a body portion can be employed as a storage device.

"The showing of motivation to combine must be clear and particular, and it must be supported by actual evidence." *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1334 (Fed. Cir. 2002), citing *In re Dembiczak*, 175 F.3d at 999. "Broad, conclusory statements regarding the teaching of the multiple references, standing alone, are not 'evidence.'" *In re Dembiczak*, 175 F.3d at 999.

While the Final Rejection is correct that "any judgment on obvious is in a sense necessarily a reconstruction based upon hindsight, the Federal Circuit requires a "rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *McGinley*, 262 F.3d at 1351; *In re Dembiczak*, 175 F.3d at 999. This is required because "[t]he genius of invention is often a combination of known elements which in hindsight seems preordained. " *McGinley*, 262 F.3d at 1351; *In re Dembiczak*, 175 F.3d at 999.

This "rigorous application" is "the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis." *In re Dembiczak*, 175 F.3d at 999; "To prevent hindsight invalidation of patent claims, the law requires some teaching, suggestion or reason to combine cited references." *McGinley*, 262 F.3d at 1351. "When the art in question is relatively simple . . . the opportunity to judge by hindsight is particularly tempting. Consequently, the tests of whether to combine references need to be applied rigorously." *Id.* As such, the teachings of Pham and Ohsawa are not properly combinable.

b. Pham teaches away from the use of FinFET as a storage transistor.

The Final Rejection, acknowledging that Ohsawa lacks the "gate" and "gate structure" limitations of independent claims 1, 23, 28, 30, 32 and 47, relies on the FinFET of Pham to meet these limitations. In doing so, the Final Rejection ignores the explicit teachings of Pham that preclude the use of its FinFET as a storage transistor, and ignores the fact that combining the FinFET of Pham with the storage transistor of Ohsawa would result in an inoperable device.

"[R]eferences that teach away [from a particular combination] cannot serve to create a prima facie case of obviousness." *McGinley*, 262 F.3d at 1353-4, citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). The Federal Circuit has also held that a modification that produces a "seemingly inoperable device" necessarily teaches away from that modification. *McGinley*, 262 F.3d at 1354, citing *In re Sponnoble*, 405 F.2d 578, 587 (CCPA 1969); *In re Gordon*, 733 F.2d 900 , 902 (Fed. Cir. 1984).

The combination of the FinFET of Pham with Ohsawa would create a "seemingly inoperable device" because the changes proposed by the Final Rejection would destroy the

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[4] As noted above, although exemplary embodiments of Appellants' invention include FinFETs and although the FinFET of Pham is relied on by the Final Office Action, Appellants' claims are not limited to FinFETs.

ability of the FinFET of Pham to operate as contemplated by the Pham disclosure. The storage transistor of Ohsawa, for example, uses a "floating body transistor cell (FBC) [which] consists of a MOSFET with its body floating electrically," which requires channel doping. (See Ohsawa, p. 1510). However, doping the Pham FinFET in this manner would destroy the ability of the FinFET to operate as contemplated by the Pham disclosure, *i.e.*, employing an *undoped* channel for its desired carrier mobility and junction characteristics (*see* Pham, Col. 1, lines 32-35 (describing the "intense channel doping" found in the prior art as undesirable because it "degrade[s] carrier mobility and junction characteristics" and proposing a FinFET that does not exhibit this drawback)).

To modify the prior art as described by the Final Rejection would render the resulting device "seemingly inoperable." The entire disclosure of Pham contemplates employing an *undoped* channel for its desired carrier mobility and junction characteristics because "intense channel doping begins to degrade carrier mobility and junction characteristics." (Pham, Col. 1, lines 34-35). This feature is not limited to one preferred embodiment, as the Final Rejection suggests; this feature is critical to the entire Pham disclosure, and the undesirability of any channel doping is explicit (*see Id.*). Therefore, Pham teaches away from Appellant's invention as a matter of law.

This proposed modification of Ohsawa is not merely "inferior," as suggested by the Final Rejection, but results in a "seemingly inoperable device" unless the combination is further modified. *In re Gurley*, cited by the Final Rejection at page 6, applies only to situations where a configuration is disclosed, yet described as undesirable. In this instance, however, the claimed configuration is *not* disclosed; therefore *In re Gurley* does not apply. Instead, Pham describes the condition of a highly-doped channel as uniformly undesirable; this view pervades the disclosure, and is not limited to the preferred embodiment as the Final Rejection suggests. The presence of a highly doped channel, required by the storage transistor of Ohsawa, therefore, makes it undesirable to combine Pham with Ohsawa in a way that would meet all the limitations of Appellant's claims.

The Final Rejection cites to a broad, conclusory statement at Pham, Col. 8-9 which states that "the invention is not limited to any particular type of integrated circuit described herein," but to interpret this as encompassing a storage transistor having a highly doped channel, *e.g.*, the storage transistor of Ohsawa, is to ignore both the language of the phrase itself, *i.e.*, that other integrated circuits have *not* been "described herein," and also the explicit teaching of Pham that a highly doped channel is undesirable. This boilerplate statement does not purport to disclose anything at all, but simply acknowledges that other "particular type[s] of integrated circuit[s]" exist; none of the "particular type[s] of integrated circuit[s]" which are actually "described herein" by Pham disclose, teach or suggest a storage transistor.

Accordingly, there is no motivation to combine Pham with Ohsawa. When confronted with the problem of configuring the storage transistor of Ohsawa, having a heavily doped channel, a person of ordinary skill would not be motivated to use the FinFET construction of Pham, because Pham is not directed toward the use of a FinFET as a storage transistor and teaches directly away from the use of a heavily doped channel to create a device suitable for use as the claimed storage transistor.

3. Kencke does not cure the deficiencies of Pham or Ohsawa

Kencke is relied upon as allegedly teaching "generating carriers through impact ionization," and source/drain regions comprising "layers of Si_xGe_{1-x} and Se_yGe_{1-y} with different band gaps." Kencke, however, fails to address any of the underlying flaws in the combination of Pham and Ohsawa, discussed in depth above. Moreover, there is no motivation to combine the impact ionization feature and plural source/drain layers of Kencke with the device of Pham, Ohsawa, or both. As such, the rejection should be reversed.

The Final Rejection also argues at page 4 that "Applicant has not established the criticality of the [Si and Ge] doses stated," and therefore, it would have been obvious to combine Kencke's disclosure of Si_xGe_{1-x} and Si_yGe_{1-y} with Pham and Ohsawa. Appellant disagrees. The burden is on the PTO to provide a motivation to combine these references. There is no obligation for the Appellant to establish that these proportions represent a critical dose; this limitation does not establish any specific "dose" of either material, or even a range of doses, but rather a variable relationship between the Silicon and/or Germanium content of the layers, i.e. "layers of Si_xGe_{1-x} and Se_yGe_{1-y} with different band gaps." In any event, the advantages of employing Silicon and Germanium in these proportions are explained at page 15 of Appellant's specification.

B. CLAIMS 8 AND 35 ARE PATENTABLE OVER OHSAWA IN VIEW OF PHAM AND FURTHER IN VIEW OF KENCKE, AND FURTHER IN VIEW HU (GROUND OF REJECTION B).

Claim 8 depends from claim 1 and claim 35 depends from claim 32. Claims 8 and 35 each further recite that "the body portion contains a heavily doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region."

As discussed above, Ohsawa, Pham and Kencke fail to teach or suggest the limitations of claims 1 and 35. The Final Rejection admits at page 4 that these references fail to teach or suggest the limitations of claims 8 and 35. Hu does not supplement the deficiencies of Ohsawa, Pham and Kencke regarding claims 1 and 32. Moreover, Hu does not teach the limitation it is being cited for.

The Final Rejection uses a buried word line 16 of Hu as the "heavily doped region" for the purposes of the claim, but ignores the fact that the heavily doped region is contained within the body portion and is a distinct element from the word line of the claimed invention of claims 8 and 35. There is no motivation to insert the word line of Hu as an element of the claimed transistor *in addition to* the existing word line of the claimed transistor. Moreover, the buried word line 16 has the same conductivity as region 14, which is not the same as the claimed invention, which requires the heavily doped region to be a different conductivity from the source/drain regions. For at least these reasons, the rejection of claims 8 and 35 is improper.

In addition, the disclosure of Ohsawa explicitly teaches away from the use of the disclosure of Hu. Ohsawa discusses the undesirability of Hu's "capacitorless DRAM cell on SOI substrate" at page 1510, because "the cell structure is complicated and requires a larger cell area than a single transistor cell." The Hu article referenced by Ohsawa at page 1510 is directed to the same disclosure as the Hu patent cited by the Final Rejection; inventors Hu and Wann authored the article, the article was published the same month as the application date for the patent, and the titles of the article and patent are nearly identical. This is one more reason why the rejections of claims 8 and 35 should be reversed.

C. CLAIMS 14-16, 38-40, AND 59-61 ARE PATENTABLE OVER OHSAWA IN VIEW OF PHAM AND FURTHER IN VIEW OF KENCKE, AND FURTHER IN VIEW OF MATSUMOTO (GROUND OF REJECTION C).

Claims 14-16, 38-40, and 59-61 depend from claims 1, 32 and 47 respectively. As discussed above, Ohsawa, Pham and Kencke fail to teach or suggest all limitations of independent claims 1, 32 and 47. Matsumoto does not cure the deficiencies of Ohsawa, Pham and Kencke, and is cited for teaching a silicide contact in a bipolar transistor.

In addition, there is no motivation to combine the additional teachings of Matumoto with the combination of Ohsawa, Pham and Kencke (a total of four different references). For at least these reasons, the rejection of claims 14-16, 38-40, and 59-61 is improper and should be reversed.

D. CLAIMS 15 AND 58 ARE PATENTABLE OVER OHSAWA IN VIEW OF PHAM AND FURTHER IN VIEW OF KENCKE, AND FURTHER IN VIEW OF TAKASU (GROUND OF REJECTION D).

Claims 15 and 58 depend from claims 1 and 47 respectively. As discussed above, Ohsawa, Pham and Kencke fail to teach or suggest all limitations of independent claims 1 and 47. Takasu does not cure the deficiencies of Ohsawa, Pham and Kencke, and is cited for teaching an insulating material with a high dielectric constant.

In addition, there is no motivation to combine the additional teachings of Takasu with the combination of Ohsawa, Pham and Kencke (a total of four different references). For at least these reasons, the rejection of claims 15 and 58 is improper and should be reversed.

E. CLAIMS 9, 10, 27, 36, 54 AND 55 ARE PATENTABLE OVER OHSAWA IN VIEW OF PHAM AND FURTHER IN VIEW OF KENCKE, AND FURTHER IN VIEW OF YU (GROUND OF REJECTION E).

Claims 9, 10, 27, 36, 54, and 55 depend from claims 1, 23, 32 and 47 respectively. As discussed above, Ohsawa, Pham and Kencke fail to teach or suggest all limitations of independent claims 1, 23, 32 and 47. Yu does not cure the deficiencies of Ohsawa, Pham and Kencke, and is cited for teaching an inert dopant in a channel region of a transistor.

In addition, there is no motivation to combine the additional teachings of Yu with the combination of Ohsawa, Pham and Kencke (a total of four different references). For at least these reasons, the rejection of claims 9, 10, 27, 36, 54, and 55 is improper and should be reversed.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: December 22, 2006

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/680,158

1. (Previously presented) A memory device comprising:

a storage transistor at a surface of a substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, wherein the first and second source/drain regions are regions of a first conductivity type, each of the first and second source/drain regions including a plurality of layers capable of generating carriers through impact ionization, and

a gate structure, wherein the gate structure wraps at least partially around the body portion;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

2. (Original) The memory device of claim 1, wherein the substrate is a silicon-on-insulator substrate.

3. (Original) The memory device of claim 1, wherein the storage transistor is a partially depleted device.

4. (Original) The memory device of claim 1, wherein the substrate is a semiconductor layer of a second conductivity type overlying a semiconductor layer of a first conductivity type.

5. (Original) The memory device of claim 1, wherein the storage transistor is a FinFET.

6. (Original) The memory device of claim 1, wherein the gate structure comprises a gate electrode, and wherein the gate electrode comprises a material from the

group consisting of P+ polysilicon, N+ polysilicon, P+ Si_xGe_{1-x}, N+ Si_xGe_{1-x}, Ti, TaN, WN, and W.

7. (Original) The memory device of claim 1, wherein the gate structure comprises a metal gate electrode.

8. (Original) The memory device of claim 1, wherein the body portion contains a heavily doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region.

9. (Original) The memory device of claim 1, wherein the body portion contains an inert dopant region heavily doped with inert ions adjacent to the first source/drain region and separated from the second source/drain region.

10. (Previously presented) The memory device of claim 9, wherein the inert dopant region has a dopant dose within the range of approximately $5x10^{12}$ atoms/cm^2 to approximately $1x10^{16}$ atoms/cm^2.

11. (Original) The memory device of claim 1, wherein the storage transistor further comprises an insulating layer between the gate structure and the body portion, and wherein the thickness of the insulating layer on a top surface of the body portion is greater than the thickness of the insulating layer on sidewalls of the body portion.

12. (Original) The memory device of claim 11, wherein the insulating layer is a material from the group consisting of silicon oxide, oxynitride, nitrided hafnium oxide, aluminum-doped hafnium oxide, hafnium oxide, aluminum oxide, zirconium oxide, tantalum pentoxide lanthanum oxide, titanium oxide, and yttrium oxide.

13. (Original) The memory device of claim 11, wherein the insulating layer is a material having a high dielectric constant.

14. (Original) The memory device of claim 1, wherein the storage transistor further comprises a higher Schottky barrier between the second source/drain region and the

body portion than a Schottky barrier between the body portion and the first source/drain region.

15. (Original) The memory device of claim 14, wherein the storage transistor further comprises a silicide layer in contact with the second source/drain region.

16. (Original) The memory device of claim 15, wherein the storage transistor further comprises a silicide layer in contact with the first source/drain region.

17. (Original) The memory device of claim 1, wherein the first and second source/drain regions are raised such that the first and second source/drain regions share a same horizontal spatial plane as the portion of the gate structure on a sidewall of the body portion.

18. (Previously presented) The memory device of claim 1, wherein the plurality of layers comprises at least one layer of a first material and at least one layer of a second material.

19. (Original) The memory device of claim 18, wherein the first and second materials have different band gaps.

20. (Original) The memory device of claim 18, wherein the plurality of layers are configured such that a first carrier type gains energy upon moving through the plurality of layers.

21. (Original) The memory device of claim 18, wherein the first and second materials have different valence band energies.

22. (Original) The memory device of claim 18, wherein the plurality of layers comprises alternating layers of Si_xGe_{1-x} and Si_yGe_{1-y}, respectively, where x is not equal to y.

23. (Original) A dynamic random access memory (DRAM) cell comprising:

a storage transistor at a surface of a silicon-on-insulator (SOI) substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the body portion containing a heavily doped region of a first conductivity type adjacent to the second source/drain region and separated from the first source/drain region, the first and second source/drain regions being regions of a second conductivity type, and

a gate structure, the gate structure wrapping at least partially around the body portion in at least two spatial planes;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

24. (Original) The DRAM cell of claim 23, wherein the body portion comprises at least one fin-shaped structure, wherein the storage transistor further comprises an oxide layer between the gate structure and the body portion, and wherein the thickness of the oxide layer on a top surface of each fin-shaped structure is greater than the thickness of the oxide layer on sidewalls of each fin-shaped structure.

25. (Original) The DRAM cell of claim 23, wherein the first and second source/drain regions are silicided differently from one another.

26. (Original) The memory device of claim 23, wherein the first and second source/drain regions have different dopant concentrations than one another.

27. (Original) The DRAM cell of claim 23, wherein the body portion comprises an inert dopant region adjacent to the first source/drain region, the inert dopant region having an amorphous dopant profile, and wherein the peak of the dopant profile is within a buried oxide layer.

28. (Original) A memory array comprising:

a plurality of memory cells, each memory cell comprising a storage transistor at a surface of a silicon-on-insulator (SOI) substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the body portion containing a heavily doped region of a first conductivity type adjacent to the second source/drain region and separated from the first source/drain region, the first and second source/drain regions being regions of a second conductivity type, and

a plurality of gates at least partially surrounding the body portion;

a bit line connected to the first source/drain region; and

a word line connected to at least one gate.

29. (Original) The memory array of claim 28, wherein the plurality of gates are interconnected.

30. (Previously presented) A semiconductor chip comprising:

a plurality of dynamic random access memory (DRAM) cells, at least one DRAM cell comprising a partially depleted storage transistor at a surface of a silicon-on-insulator (SOI) substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the body portion comprising at least one fin-shaped structure and a region of a first conductivity type adjacent to the second source/drain region, the first and second source/drain regions being regions of a second conductivity type and each of the first and second source/drain regions including a plurality of layers capable of generating carriers through impact ionization, and

a gate structure, the gate structure wrapping at least partially around each fin-shaped structure;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

31. (Original) The semiconductor chip of claim 30, wherein the gate structure wraps uninterruptedly around three sides of each fin structure.

32. (Previously presented) A processor system comprising:

a processor coupled to a memory device, the memory device comprising a plurality of memory cells, each memory cell comprising a storage transistor at a surface of a substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the first and second source/drain regions being regions of a first conductivity type and each of the first and second source/drain regions including a plurality of layers capable of generating carriers through impact ionization, and

a gate structure, the gate structure wrapping at least partially around the body portion;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

33. (Original) The processor system of claim 32, wherein the substrate is a silicon-on-insulator substrate.

34. (Original) The processor system of claim 32, wherein the storage transistor is a FinFET.

35. (Original) The processor system of claim 32, wherein the body portion contains a heavily doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region.

36. (Original) The processor system of claim 32, wherein the body portion contains an inert dopant region heavily doped with inert ions adjacent to the first source/drain region and separated from the second source/drain region.

37. (Original) The processor system of claim 32, wherein the storage transistor further comprises an oxide layer between the gate structure and the body portion, and

wherein the thickness of the oxide layer on a top surface of the body portion is greater than the thickness of the oxide layer on sidewalls of the body portion.

38. (Original) The processor system of claim 32, wherein the storage transistor further comprises a higher Schottky barrier between the second source/drain region and the body portion than a Schottky barrier between the body portion and the first source/drain region.

39. (Original) The processor system of claim 38, wherein the storage transistor further comprises a silicide layer in contact with the second source/drain region.

40. (Original) The processor system of claim 39, wherein the storage transistor further comprises a silicide layer in contact with the first source/drain region.

41. (Original) The processor system of claim 32, wherein the first and second source/drain regions are raised such that the first and second source/drain regions share a same horizontal spatial plane as the portion of the gate structure on a sidewall of the body portion.

42. (Previously presented) The processor system of claim 32, wherein the plurality of layers comprises at least one layer of a first material and at least one layer of a second material.

43. (Original) The processor system of claim 42, wherein the first and second materials have different band gaps.

44. (Original) The processor system of claim 42, wherein the plurality of layers are configured such that a first carrier type gains energy upon moving through the plurality of layers.

45. (Original) The processor system of claim 42, wherein the first and second materials have different valence band energies.

46. (Original) The processor system of claim 42, wherein the plurality of layers comprises alternating layers of Si_xGe_{1-x} and Si_yGe_{1-y}, respectively, where x is not equal to y.

47. (Original) A transistor device comprising:

a first source/drain region of a first conductivity type;

a second source/drain region of a first conductivity type;

a body portion for storing charge, the body portion protruding from a surface of a substrate, the body portion being located between the first and second source/drain regions, the body portion including a doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region; and

a gate structure wrapping around the body portion in at least two spatial planes.

48. (Original) The transistor device of claim 47, wherein the substrate is a silicon-on-insulator substrate.

49. (Original) The transistor device of claim 47, wherein the substrate is a semiconductor layer of a second conductivity type overlying a semiconductor layer of a first conductivity type.

50. (Original) The transistor device of claim 47, wherein the storage transistor is a FinFET.

51. (Original) The transistor device of claim 47, wherein the gate structure comprises a gate electrode, and wherein the gate electrode comprises a material from the group consisting of P+ polysilicon, N+ polysilicon, P+ Si_xGe_{1-x}, N+ Si_xGe_{1-x}, Ti, TaN, WN, and W.

52. (Original) The transistor device of claim 47, wherein the gate structure comprises a metal gate electrode.

53. (Previously presented) The transistor device of claim 47, wherein the region of a second conductivity type has an implant dose of between approximately $5x10^{12}$ atoms/cm^2 to approximately $1x10^{14}$ atoms/cm^2.

54. (Original) The transistor device of claim 47, wherein the body portion contains an inert dopant region heavily doped with inert ions adjacent to the first source/drain region and separated from the second source/drain region.

55. (Previously presented) The transistor device of claim 54, wherein the inert dopant region has a dopant dose within the range of approximately $5x10^{12}$ atoms/cm^2 to approximately $1x10^{16}$ atoms/cm^2.

56. (Original) The transistor device of claim 47, further comprising an insulating layer between the gate structure and the body portion, and wherein the thickness of the insulating layer on a top surface of the body portion is greater than the thickness of the insulating layer on sidewalls of the body portion.

57. (Original) The transistor device of claim 56, wherein the insulating layer is a material from the group consisting of silicon oxide, oxynitride, nitrided hafnium oxide, aluminum-doped hafnium oxide, hafnium oxide, aluminum oxide, zirconium oxide, tantalum pentoxide lanthanum oxide, titanium oxide, and yttrium oxide.

58. (Original) The transistor device of claim 56, wherein the insulating layer is a material having a high dielectric constant.

59. (Original) The transistor device of claim 47, further comprising a higher Schottky barrier between the second source/drain region and the body portion than a Schottky barrier between the body portion and the first source/drain region.

60. (Original) The transistor device of claim 59, further comprising a silicide layer in contact with the second source/drain region.

61. (Original) The transistor device of claim 60, further comprising a silicide layer in contact with the first source/drain region.

62. (Original) The transistor device of claim 47, wherein the first and second source/drain regions are raised such that the first and second source/drain regions share a

same horizontal spatial plane as the portion of the gate structure on a sidewall of the body portion.

63. (Original) The transistor device of claim 47, wherein the first and second source/drain regions each include a plurality of layers, and wherein the plurality of layers comprises at least one layer of a first material and at least one layer of a second material.

64. (Original) The transistor device of claim 63, wherein the first and second materials have different band gaps.

65. (Original) The transistor device of claim 63, wherein the plurality of layers are configured such that a first carrier type gains energy upon moving through the plurality of layers.

66. (Original) The transistor device of claim 63, wherein the first and second materials have different valence band energies.

67. (Original) The transistor device of claim 63, wherein the plurality of layers comprises alternating layers of Si_xGe_{1-x} and Si_yGe_{1-y}, respectively, where x is not equal to y.

Claims 68-110 (Canceled).

APPENDIX B

A copy of evidence entered by or relied upon by the examiner that is relevant to this appeal is attached hereto. Exhibits 1, 2 and 4-7 were first entered by the examiner in the Office Action mailed February 1, 2005. Exhibit 3 was first entered by the examiner in the Office Action mailed January 4, 2006.

Exhibit 1: "Memory Design Using One-Transistor Gain Cell on SOI" by Ohsawa et al. (2002 IEEE International Solid State Circuits Conference)

Exhibit 2: U.S. Patent No. 6,838,322 to Pham et al.

Exhibit 3: 6,313,486 to Kencke et al.

Exhibit 4: U.S. Patent No. 5,448,513 to Hu et al.

Exhibit 5: U.S. Patent No. 6,806,537 to Matsumoto et al.

Exhibit 6: U.S. Patent No. 5,307,305 to Takasu

Exhibit 7: U.S. Patent No. 6,221,724 to Yu et al.

APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.

Memory Design Using a One-Transistor Gain Cell on SOI

Takashi Ohsawa, Katsuyuki Fujita, Tomoki Higashi, Yoshihisa Iwata, Takeshi Kajiyama, Yoshiyuki Asao, and Kazumasa Sunouchi

***Abstract*—A 512-kb memory has been developed featuring a one-transistor gain cell of size $7F^2(F = 0.18\ \mu m)$ on SOI. The cell named the floating body transistor cell (FBC) has the ability to achieve a $4F^2$ cell using self-aligned contact technologies and is proved to be scalable with respect to a cell signal. A basic operation was verified by device simulation and hardware measurement. An array driving method is disclosed which makes selective write possible. A cell signal sensing system consisting of a pair of reference cells written opposite data and comparing the combined current with the doubled cell current is shown to be robust against cell parameter variations in process and temperature. A random access time of 40 ns was simulated. Nondestructive readout and C_b/C_s free signal development drastically improve cell efficiency.**

***Index Terms*—Capacitor-less DRAM, DRAM, embedded memory, floating body transistor cell, gain cell, nondestructive readout, silicon-on-insulator technology.**

I. INTRODUCTION

THE conventional one-transistor and one-capacitor DRAM cell faces a serious problem as the device feature size shrinks, because new material such as high dielectric constant film is needed for a stacked capacitor [1] or a high aspect ratio trench is required for a trench capacitor combined with a vertical shape access transistor [2]. To circumvent this, several new approaches are being pursued. One is a gain cell using a stacked tunnel transistor [3], and the other is a magnetic random access memory [4], [5]. However, the former requires new device structures and the latter introduces new material into a MOS process, implying that it takes a long time for both to be phased in a productive large-scale memory.

This memory design is based on a single-transistor gain cell which is smaller, less complex to make and more scalable down to sub-0.1-μm generations than the existing DRAM cells, without resorting to new material and device structure. This cell named the floating body transistor cell (FBC) consists of a MOSFET with its body floating electrically. A MOSFET formed on partially depleted silicon-on-insulator (PD-SOI) is one of the candidates to realize the FBC [6]. The number of majority carriers (holes for nFET) is changed in write operations and a different drain current depending on the number due to the body effect is read and sensed. The idea that the SOI transistor floating body can be exploited as an electric charge storage node of a memory unit is old. Tack *et al.* disclosed the concept in 1990 but failed to develop a selective write method using a wordline and a bitline electrically, which is essential for realizing a memory device and stayed in the idea of a photodetector device [7]. In 1993, Wann and Hu presented an idea of a capacitor-less DRAM cell on SOI which also uses the floating body of an SOI transistor, and the write selectivity is achieved through a write MOS transistor which is merged into the cell transistor [8]. Thus, the cell structure is complicated and requires a larger cell area than a single transistor cell. We have developed the idea of a truly single-transistor gain cell on SOI which is electrically controlled by a wordline and a bitline, disclosing for the first time a method to write data selectively and hold them stably, a method to sense the read current difference, and design benefits such as scalability, high cell efficiency, and so on.

Section II explains what the FBC looks like and how it works. A cell structure and an array architecture are shown. Operational waveforms which guarantee the selective write and the data hold is disclosed. In Section III, basic operations are verified by device simulation. A scalability of the FBC is also discussed. Window narrowing of the data "1" and the data "0" drain currents is measured to predict retention time of the FBC in Section IV, where the bitline disturb condition is checked and an optimum operational condition is proposed. In Section V, an implementation of the FBC to a 512-kb memory is disclosed. We focus on a sense amplifier design and a reference cell design. SPICE simulation results are also shown. Finally, we summarize the features of the FBC and make some comments on future work to be done.

II. PRINCIPLE OF THE FBC

The FBC consists of a MOSFET whose body is electrically floating and is used as a storage node of electric charge. We have chosen an nFET formed on PD-SOI as a candidate to realize the concept. Fig. 1 explains a principle of the FBC. The source of the FBC is connected to 0 V (GND), the drain to a bitline (BL), and the gate to a wordline (WL). To write data, the nFET is operated in saturation, leading to impact ionization which injects holes into the body. This is defined as data state "1." To write data "0," the pn junction between the body and the drain is forward-biased, ejecting the stored holes from the body. To read the data, the nFET is operated in a linear region so as to keep the data state "0" from being violated by impact

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0018-9200/02$17.00 © 2002 IEEE

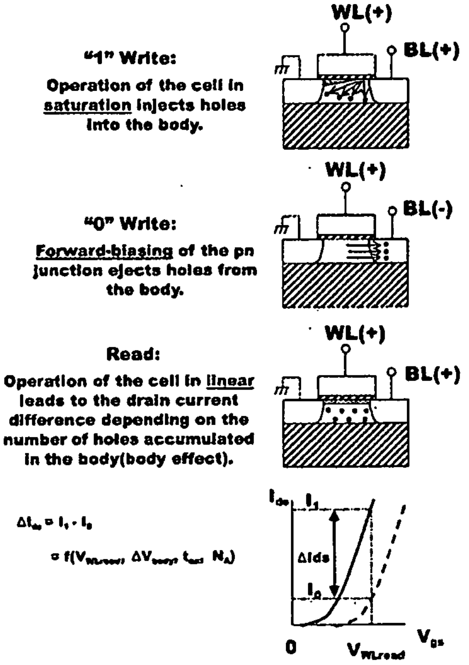

WL(+)
"1" Write:
Operation of the cell in saturation injects holes into the body.
BL(+)
WL(+)
"0" Write:
Forward-biasing of the pn junction ejects holes from the body.
BL(-)
WL(+)
Read:
Operation of the cell in linear leads to the drain current difference depending on the number of holes accumulated in the body(body effect).
BL(+)
$\Delta I_{ds} = I_1 - I_0$
$= f(V_{WLread}, \Delta V_{body}, t_{ox}, N_A)$
I_{ds}
I_1
ΔIds
I_0
0
V_{WLread}
V_{gs}

Fig. 1. Principle of the FBC.

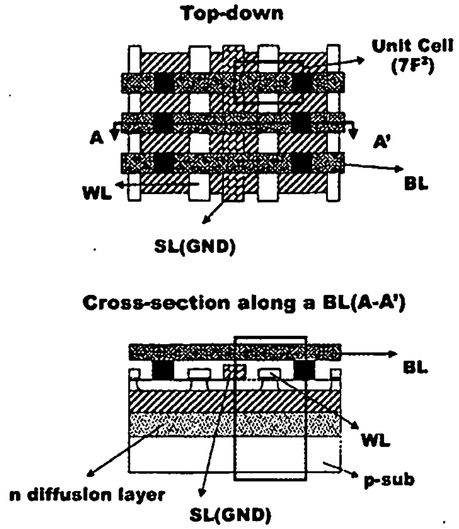


Fig. 2. Device structure and the arrangement of the FBC.

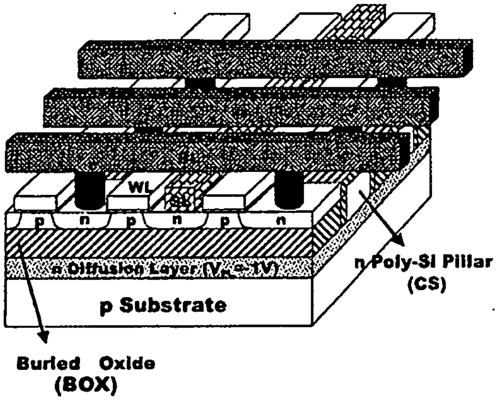


Fig. 3. Bird's eye view of the FBC.

ionization, leading to a drain current difference due to the body effect depending on the number of holes stored in the body. This difference can be read and sensed. The drain current difference ΔI_{ds}, which is a current for the data state "1" I_1 minus a current for the data state "0" I_0, is a function of the WL voltage during read, the body potential difference between the data state "1" and the "0" ΔV_{body}, the gate oxide thickness t_{ox}, and the acceptor concentration in the body N_A. The FBC is volatile and needs to be refreshed, because holes are generated in the body of the data state "0" through the pn junction reverse-bias leakage current between the body and the source/drain and they need to be bailed out in order to maintain the difference in the number of holes between the data "1" and the data "0."

Fig. 2 shows the device structure and the cell arrangement of the 512-kb memory we designed by using the FBC. The upper part is the top-down view and the lower part is the cross-sectional view cut along a BL (A-A'). The two bold rectangles in the figure define a 1-b unit cell. The gate of the cell transistor forms a WL. The source of the cell transistor is connected to a source line (SL) which runs along WLs. The drain is connected to a BL which runs perpendicular to WLs and SLs. The drain and the source of the cell transistor are shared by two adjacent cells and if both the SL contact and the BL contact are self-aligned to the WL, $4F^2$ cell size is achieved. In this memory design, however, we relaxed the size to $7F^2 (F = 0.18\ \mu m)$ using aligned contacts for the both. Both the channel length and the width are 0.18 μm and the gate oxide thickness is 60 Å. The top silicon film thickness is 1500 Å and the buried oxide (BOX) thickness is 2000 Å. Fig. 3 is a bird's eye view of the FBC. Cells are separated by pn junction in a BL direction, while they are separated by shallow trench isolation (STIs) in a WL direction. Within the STI, a poly-silicon pillar which is doped n-type is placed and is electrically connected to an n-type diffusion layer spread under the BOX which is biased at −1 V from periphery. The pillar forms a capacitor coupled to the body which accumulates holes there, thus, it serves as a stabilizing capacitor (CS) or stabilizer which helps increase the signal and the retention time as well. Fig. 4 explains how the pillar is implemented into the cell structure. The left two parts are the cell array cross sections along a BL and a WL. When you look at the along-WL cross section, you see two STI regions and there are two poly-silicon pillars within them. The dielectric material between the pillar and the body is SiO_2 and the thickness is set to × 2 with respect to the gate oxide thickness which is 60 Å. The height of the pillar is set at the middle of the top silicon film, making the capacitance of the stabilizer about 40% of the gate capacitance C_{OX}. A more detailed explanation for the role of the CS is to be given in the next section.

An array driving method is disclosed in Fig. 5 which makes possible a selective write and read and a stable data hold. In this figure, which is only a hand-writing schematic chart, two read modify write cycles are described. The first cycle is for

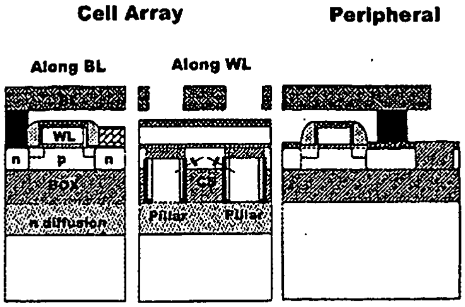


Fig. 4. Cross-sectional view of the cell array and the periphery.

a "1" read modify "0" write and the second is for the opposite data polarity. For reading the data "1" or the "0," the corresponding WLs are raised, followed by the body potentials' going up through a capacitive coupling between the gate and the body. However, depending on initially held levels, the body potentials for the corresponding data cells reach different levels, letting the "1" cell's body potential higher than the "0" cell's one. So the two transistors have different threshold voltages ($V_{\rm th}$'s) due to the body effect, the data "1" cell's $V_{\rm th}$ being lower than the data"0" cell's one. Also, if a constant current is supplied from the BL to GND through the transistors, different voltages appear on the two BLs: one is connected to the data "1" cell and the other to the data"0" cell. This difference can be read and sensed by sense amplifier circuits. For writing the data "0," the BL is lowered to a negative level, making the pn junction forward-biased between the body and the drain and holes are ejected from the body, the body potential trailing immediately after the BL voltage and reaching the "0" write BL voltage plus about V_f, which is the turn-on voltage of the pn junction $\sim$ 0.7 V. For writing the data "1," the BL level is raised to bias the cell at saturation, the holes being injected into the body due to impact ionization and the body potential going up and reaching about V_f. After writing the both data, the WLs are shut down to a negative holding level to let both body potentials be pushed back and held at reverse-bias conditions of the pn junction again through the capacitive coupling between the gate and the body. Finally, the BLs are returned to GND, completing the cycles and defining the holding states. The order to return the WL first and the BL afterwards is important to obtain a large signal, and the reason for this will be explained in the next section.

The selectivity of writing the data "1" and reading is clearly understood because the only cross-point cell is activated by raising a WL and a BL. On the other hand, since many cells are connected to a BL, the selectivity of writing the data "0" is not trivial, and the mechanism to realize the "0" write selectivity and conditions to avoid the BL disturb during the "0" write operation need to be clarified. Fig. 6 explains the reason why the "0" write selectivity is achieved by the basic operational waveforms shown in Fig. 5. We assume that two cells represented by the upper and the lower curves are connected to a same BL and that they have been written "1" as is shown at the first cycle in Fig. 6. In the second cycle, the upper cell is assumed to be selected to write "0," while the lower cell is not selected. The potential of the selected "1" cell's body rises high by the WL coupling, while that of the nonselected "1" cell's body remains low. So, when the BL is lowered for writing the "0" data, the potential difference between the BL and the selected "1" cell's body can become much larger than the turn-on voltage V_f of the pn junction ($\sim$ 0.7 V), while the difference between the BL and the nonselected "1" cell's body stays less than V_f, letting the hole current from the selected "1" cell's body to the BL much larger than that of the nonselected "1" cell's body. This current difference is large enough to make the selectivity of the "0" write whose duration is as short as a few nanoseconds.

III. DEVICE SIMULATION RESULTS OF THE FBC

To verify the basic operation of the FBC, a transient analysis of a two-dimensional (2-D) device simulation was performed. We used a simulator *DSStation* which had been developed internally. Fig. 7 shows the external waveforms for the WL and the BL and the simulated body potential which is represented by the hole quasi-Fermi level at the center of the body. The following device parameters were used: L(channel length) $=$ W(channel width) $=$ 0.18 μm, $t_{\rm OX}$(gate oxide thickness) $=$ 60 Å, $t_{\rm Si}$(top silicon film thickness) $=$ 1000 Å, $t_{\rm BOX}$(buried oxide thickness) $=$ 2000 Å, N_A(body acceptor concentration) $= 5 \times 10^{17}$ cm^{-3}. A poly silicon gate was used which was doped n-type. The capacitance of the stabilizer was $0.3 \times C_{\rm OX}$. This capacitor was added as a back gate in a double-gate SOI transistor structure ($t_{\rm OX2}$ $=$ 200 Å) as is shown in Fig. 8(a) in order to keep the simulation from going beyond the 2-D calculation. Therefore, this structure was only used for the purpose of adding the capacitor coupled to the body within the 2-D simulation context and did not necessarily reflect the actual device structure.

The analysis starts with an equilibrium state of the "0" write. Subsequently, the "0" data is held at 4 ns and read from 6 to 8 ns. Then the opposite data "1" is written from 10 to 20 ns by raising the BL level to bias the cell at saturation, the body potential rising up and reaching a saturated level which is about 0.8 V $\sim$ $V_f + 0.1$ V. The "1" write speed is estimated about 5 ns. Then the data "1" is held at 24 ns followed by the reading of the data from 26 to 28 ns, and the opposite data "0" is written by lowering the BL level at -0.9 V, the pn junction being forward-biased and the body potential following the BL voltage and reaching a saturated level which is about -0.2 V $\sim$ $-0.9\ {\rm V} + V_f$. The "0" write speed is estimated to be about 4 ns. After the data "0" is held at 44 ns, the data is read from 46 to 48 ns.

Fig. 9 shows the resultant read signal during the read operations. The I_1 is the drain current for the data "1" simulated from 26 to 28 ns and plotted against the WL voltage, while I_0 is the drain current for the data "0" from 46 to 48 ns. The threshold voltage difference of 200 mV is observed and the current ratio of 2 is achieved if the cells are read at 0.8 V for the WL voltage at read.

In Fig. 8, there are two nFETs: (a) one for L $=$ 0.18 μm which was implemented into the memory design and (b) the other for L $=$ 0.07 μm which is just the linear shrink of the $L = 0.18$ μm device for the future. The acceptor concentration

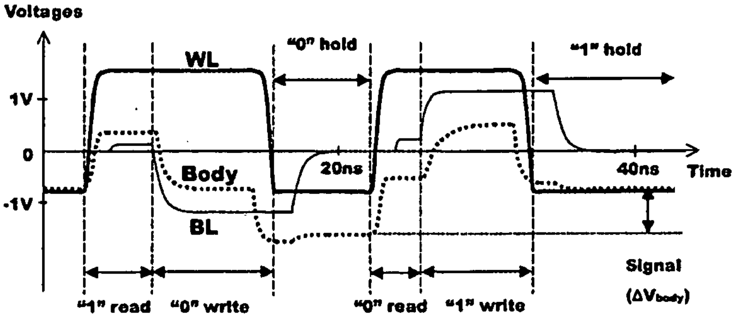


Fig. 5. Schematic view of the cell driving method.

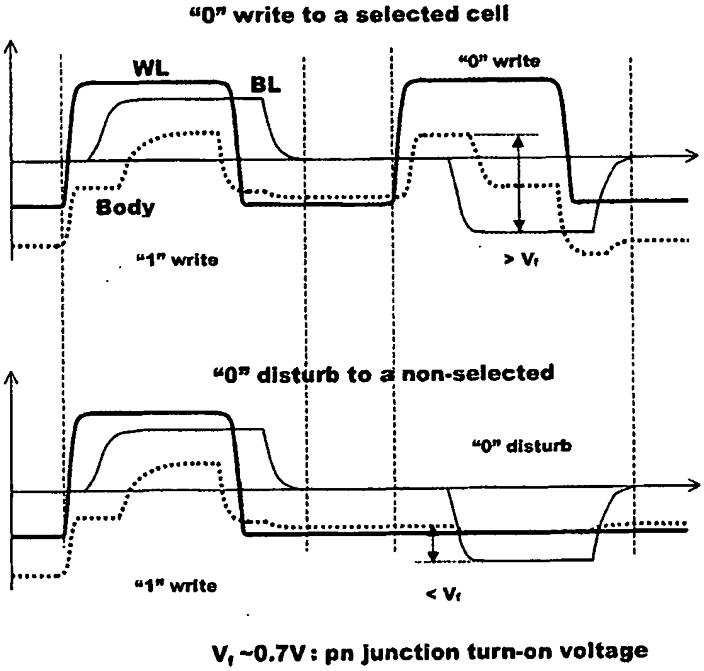

"0" write to a selected cell
WL
BL
Body
"1" write
"0" write
> V_f
"0" disturb to a non-selected
"0" disturb
"1" write
< V_f
V_f ~0.7V: pn junction turn-on voltage

Fig. 6. Schematic explanation of the "0" write selectivity.

of the $L = 0.07$ μm device is heightened so as to have the same amount of the body effect as the $L = 0.18$ μm device by compensating the decrease of the effect due to the t_{OX} thinning. The two FBCs for different generations are simulated under the same driving voltage condition. Though the constant voltage condition leads to a higher electric field for the $L = 0.07$ μm device than $L = 0.18$ μm device does, we just performed this comparison in order to see whether the FBC read signal is independent of the device feature size as a primary characteristic coming from its purely geometrical structure.

Fig. 10 shows the simulation results for Fig. 8(a) of the $L = 0.18$ μm device structures. The upper part is the threshold voltage difference v.s. t_{OX2}/t_{OX1} which is the stabilizer capacitance normalized by the gate oxide capacitance C_{OX}. There are two curves, one (WL-first) corresponds to the situation where the WL is returned to the holding level before the BL is reset to GND after writing data and the other (BL-first) corresponds to the situation where the BL is reset to GND before the WL is returned to the holding level. The lower part is the BL low level V_{BLL} during the data "0" write for the both cases (in this simulation, the V_{BLL} for the case WL-first was turned out to be the same as that for the case BL-first.). The reason why we set V_{BLL} the shallower (smaller absolute value) for the thinner t_{OX2} is that the deeper V_{BLL} than this level disturbs the unselected "1" data under the condition of the constant WL holding voltage V_{WLL}(-1.5 V in this simulation), and this limit level becomes the shallower as the t_{OX2} decreases, because the thinner t_{OX2} makes the potential of the "1" data cell's body at hold the shallower for the constant V_{WLL}. The threshold voltage difference for the WL-first is larger than that for the BL-first. This is because for the BL-first case the low body potential raises seriously when the BL returns to GND after the "0" write. This is explained by the fact that the holes piles up during the BL reset operation because the cell passes

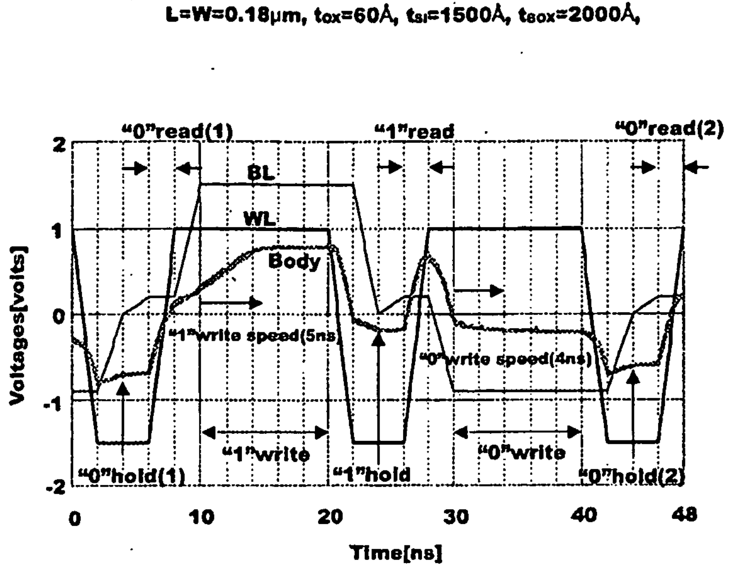


Fig. 7. Transient analysis result of the device simulation for the body potential of the FBC(L = 0.18 μm).

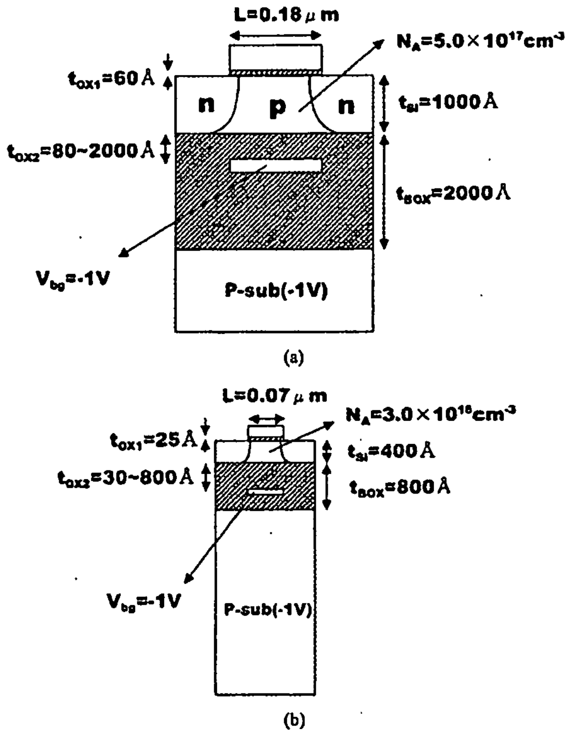


Fig. 8. Device structure used for the device simulation. (a) L = 0.18 μm. (b) L = 0.07 μm.

through saturation after "0" write and furthermore that the p-type body's neutral region is surrounded three faces by the source, the channel and the drain all n-type and they strongly couples to the body when the drain voltage returns up to GND. So the WL-first operation for the precharge is more preferable. The signal is observed to increase as the stabilizing capacitance increases. The most right point in Fig. 10(b) correspond to the case t_{OX2} = 2000 Å which is just the simple SOI structure without the stabilizer because this t_{OX2} is equal to the t_{BOX}. The signal increases by more than 50% by adding the stabilizer whose capacitance is 30% of the C_{OX} or more. The reason can be understood by looking at the device simulation waveforms in Fig. 7. The body potential difference just after the write is seen about 1 V. However, the difference decreases down to about 400 mV at hold. This is due to two causes: 1) the asymmetrical capacitive coupling from the gate to the body experienced toward the data "1" holding and the data "0" holding and 2) the deteriorating capacitive coupling to the body from the BL during the BL reset to GND. The former reason is based on the situation that the source level of the nFET is different between the "0" cell and the "1" cell during the WL returning to the V_{WLL} and that the capacitor between the gate and the body appears only when the channel disappears. This asymmetry can be avoided if the BL is reset before the WL shuts down, but this sequence has another effect to decrease the signal as was explained before. The addition of a capacitor which is coupled to a fixed voltage node to the body can mitigate these two causes, contributing to increase the signal.

Fig. 11 shows the simulation results for Fig. 8(b) of the $L =$ 0.07 μm device structures. The threshold voltage difference of $L = 0.07$ μm device is observed to be exactly the same as that of $L = 0.18$ μm device, especially for the WL-first case, proving that the ΔV_{th} is completely scalable under the constant voltage operation. In an actual scaling, the decrease of the operational voltage is also indispensable in order to keep the electrical field strength constant. This voltage scaling inevitably leads to the decrease of ΔV_{th} in the same scaling factor of the device and the voltage shrink. However, the current signal expressed by $\Delta Ids = (W/L)(\varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}})\mu_{\mathrm{eff}} \cdot \Delta V_{\mathrm{th}} \cdot V_{\mathrm{BLR}}$ can be kept constant if V_{BLR} which is a BL voltage to read the data is about 0.2 V

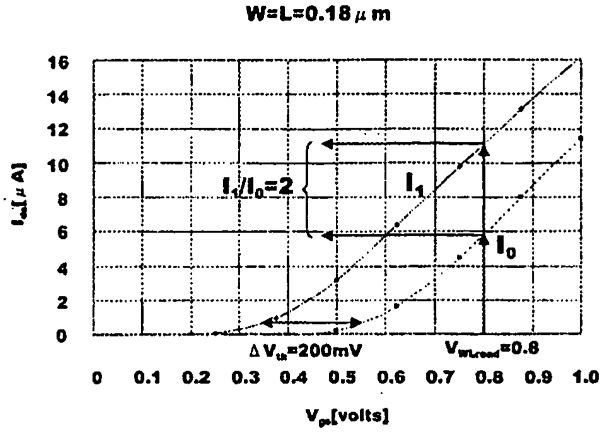
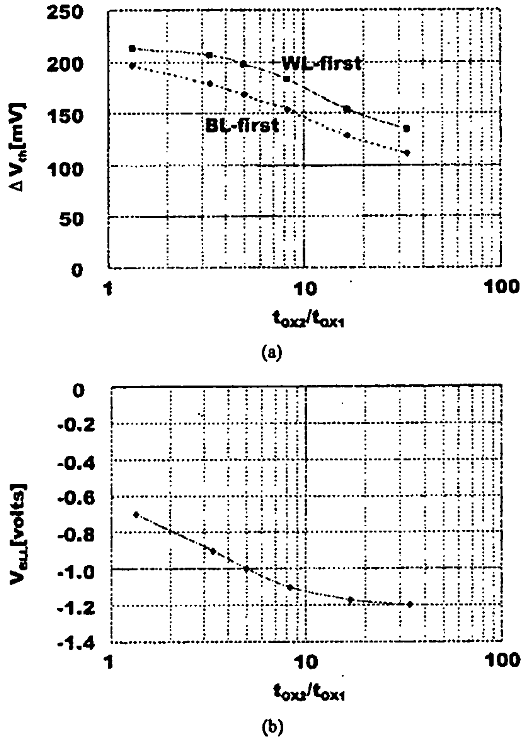


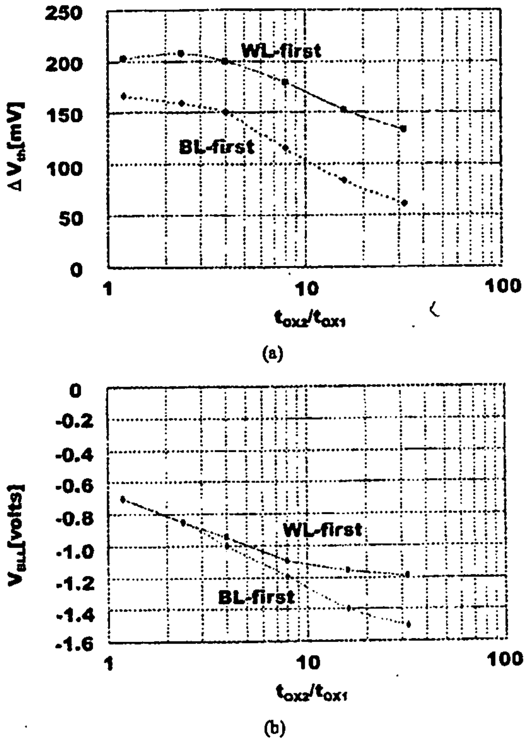
Fig. 9. Transient analysis result of the device simulation for the read currents of the FBC (L = 0.18 μm).



(a)

(b)

Fig. 10. Effect of the stabilizing capacitance on the signal of the FBC (L = 0.18 μm): (a) the signal and (b) the BL low level during the "0" write.



(a)

(b)

Fig. 11. Effect of the stabilizing capacitance on the signal of the FBC(L = 0.07 μm): (a) the signal and (b) the BL low level during the "0" write.

and is considered a constant of generation, where ε_{ox} is the permittivity of SiO$_2$ and μ_{eff} is the effective mobility of electron.

Fig. 12 is for another set of the cell device parameters which can enhance the signal. The gate oxide thickness t_{OX1} is increased from 60 to 80 Å and the acceptor concentration of the body is also increased from 5.0×10^{17} cm^{-3} to 1.0×10^{18} cm^{-3}. The top silicon film thickness t_{Si} is decreased from 1000 to 600 Å. The first two changes contribute to increase an extent of the body effect and the last change to decrease the capacitive coupling between the BL and the body. The signal is nearly doubled ($\Delta V_{th} \sim 450$ mV) and even the simple SOI structure without the stabilizer can have a 250-mV threshold voltage difference. This situation is attractive especially for embedded memory applications, because the cell structure is the same as the transistor used in Logic LSIs, making the process for the FBC compatible with Logic device ones.

IV. HARDWARE MEASUREMENT RESULTS OF THE FBC

Since the 512-kb memory hardware is in fabrication now, we tried to predict the memory's retention time by measuring the SOI transistor's drain current change with time. We assume that the retention time of the memory corresponds to the time when a window between the drain currents of the data "1" and that of the data "0" is narrowed half of its initial value. This prediction was made by measuring a single transistor the size of $L = 0.18$ μm and $W = 10$ μm with the body connected to a wiring leading to a probing pad. The wiring was cut short by laser so that the capacitance coupled to the body be adjusted equal to about C_{OX}. The charge holding capacitance, the junction leakage current including the gate induced drain leak (GIDL), the gate to the body capacitance and the drain to the body capacitance are all supposed to be proportional to the channel width. So if we neglect narrow channel effects, the primary characteristics of the retention time of the FBC implemented in the actual memory is expected to be the same as the one of the long channel transistor. Other device parameters are as follows: t_{OX1} = 60 Å, t_{Si} = 1500 Å, and t_{BOX} = 4000 Å.

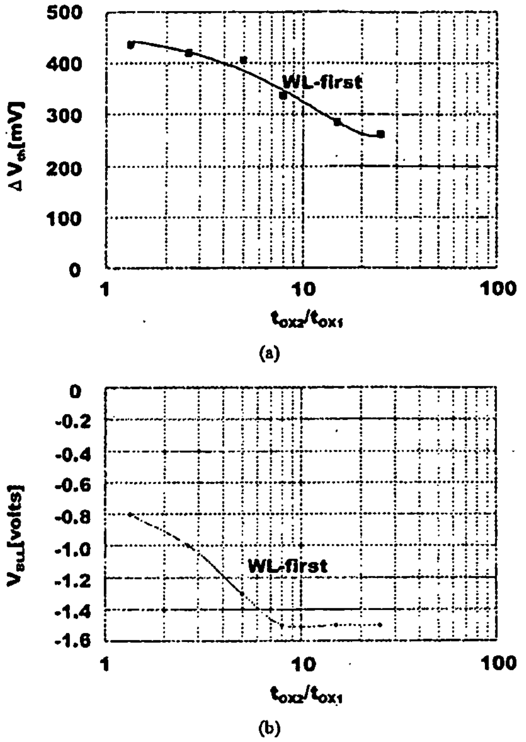


Fig. 12. Example of another cell's device parameter set which enhances the signal for the FBC (L = 0.18 μm): (a) the signal and (b) the BL low level during the "0" write.

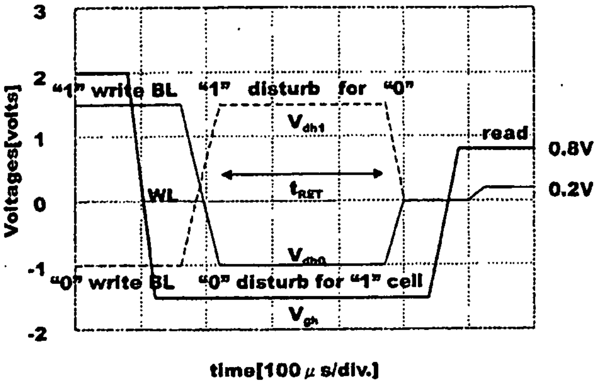


Fig. 13. External waveforms to measure the retention time for the data hold state.

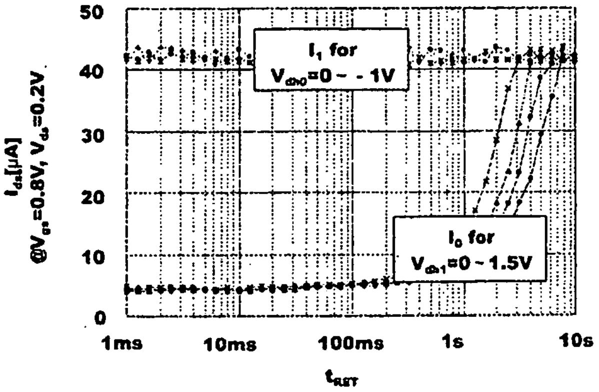


Fig. 14. Retention time measurement of the FBC (W/L = 10 μm/0.18 μm) for the data hold state at $V_{\mathrm{gh}} = -1.5$ V and 30 °C.

Fig. 13 is the external WL and BL to measure the drain current window of the transistor between the data "1" and the data "0." Initially the data "1" or the data "0" is written and afterwards the cells are exposed to the opposite BL polarities to check the worst case conditions of the BL disturb among various access data patterns. The BL disturb voltages, V_{dh1} and V_{dh0}, are changed to see the extent to which the window narrowing is affected by the BL disturb. If the dynamic transition effect of the BL can be considered as accumulation of static effect of each BL amplitude, this measurement reflects the worst case condition including BL cycling during the data hold, because the transient BL amplitude is always smaller than $V_{\mathrm{dh0}} = -1$ V and $V_{\mathrm{dh1}} = 1.5$ V. The WL holding level V_{gh} is also changed. After t_{RET} elapses, currents corresponding to the both cell data are read by raising the WL to 0.8 V and the BL to 0.2 V. This measurement was performed using a memory tester by observing the current at the end of the cycle after the elapse of t_{RET}, so every data point at different t_{RET} was obtained from a different measurement with a different t_{RET}.

Fig. 14 is the measured data at 30 °C and $V_{\mathrm{gh}} = -1.5$ V. There are two groups, one the larger current group I_1 which includes the currents corresponding to the data "1" with three different V_{dh0}'s (from 0 to -1 V with the increment of -0.5 V) and the other being the smaller current group I_0 which includes the currents corresponding to the data "0" with four different V_{dh1}'s (from 0 to 1.5 V with the increment of 0.5 V). The initial drain current ratio I_1/I_0 is about 10 and is much larger than that obtained by the device simulation in Fig. 9, which is 2. In the actual device, the threshold voltage might have been higher than the device simulation transistor's one for some reasons. So under the condition that $V_{\mathrm{WLread}} = 0.8$ V, the measured drain currents for the data "1" and the "0" are smaller but the ratio becomes larger than the device simulation case. The ratio can be 10 depending on the actual V_{th} difference between the both data. The threshold voltage difference of the hardware transistor between the data "1" and the "0" was found to be about 0.1 V. And the actual device's dimension is $W/L =$ 10 μm/0.18 μm, while the device simulation I_{ds} corresponds to $W/L = 0.18$ μm/0.18 μm. Therefore, the current drivability of the hardware is about 55 times higher than that of the device simulation transistor if the same gate overdrive is applied. But the hardware current is less than five times the simulated one, showing that the hardware transistor operated under a subthreshold condition at $V_{gs} = 0.8$ V.

We observe in Fig. 14 that I_1 never degrades, while I_0 degrades as t_{RET} increases. This is because holes are generated in the body due to the junction leak current and the data "0" state which is nonequilibrium with a smaller number of holes than the equilibrium is affected so as to be approaching the data state "1." Also, the retention time degrades as the BL disturbing voltage V_{dh1} increases. This is explained by the increase in the GIDL. The retention time of about 1 s is obtained for $L = 0.18$ μm at

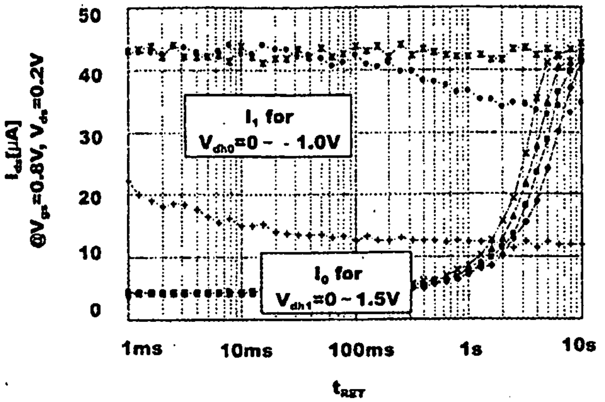


Fig. 15. The retention time measurement of the FBC (W/L = 10 μm/ 0.18 μm) for the data hold state at $V_{gh} = -0.5$ V and 30 °C.

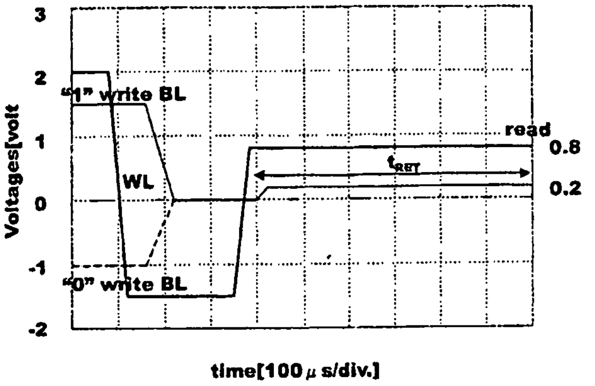


Fig. 17. The external waveforms to measure the retention time for the data read state to check the nondestructivity of read.

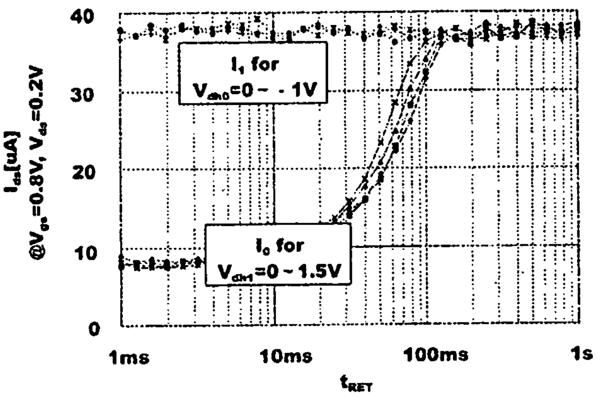


Fig. 16. The retention time measurement of the FBC (W/L = 10 μm/ 0.18 μm) for the data hold state at $V_{gh} = -1.5$ V and 85 °C.

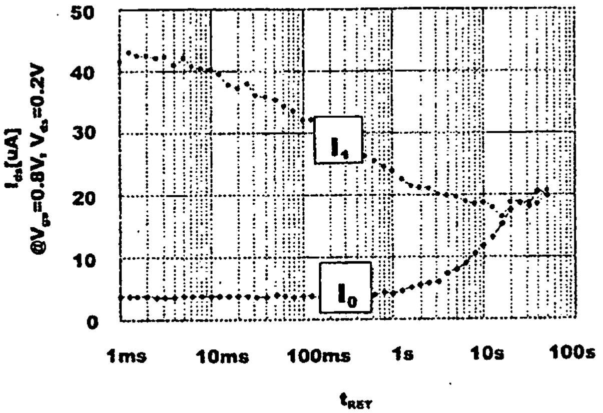


Fig. 18. The retention time measurement of the FBC (W/L = 10 μm/ 0.18 μm) for the data read state at $V_{gh} = -1.5$ V and 30 °C.

30 °C. Fig. 15 is the measured data at 30 °C and $V_{gh} = -0.5$ V. Contrary to Fig. 14, where $V_{gh} = -1.5$ V, two curves in the group I_1 degrade that correspond to the deeper V_{dh0} which are -1.0 V and -0.5 V. This is the "0" disturb which occurs because of the shallow WL holding voltage V_{gh} which is set at -0.5 V. We need to hold the WL deep enough to avoid the "0" disturb and this necessary holding level becomes deeper as the stabilizing capacitance C_S becomes larger. By comparing Fig. 15 with Fig. 14, we realize that the shallower WL hold voltage improves the retention time if we can avoid the "0" disturb. This deterioration of the retention time due to a deeper WL hold voltage is again explained by the increase in GIDL. Fig. 16 shows the measured data at 85 °C and $V_{gh} = -1.5$ V. We obtain about 50 ms of retention time for $L = 0.18$ μm at 85 °C. These retention time numbers can be improved by using a higher performance SOI structure with a thinner t_{Si} together with a higher quality SOI substrate.

One of the most important features of the FBC is the nondestructive readout. This comes from the expectation that the number of the stored holes is not affected by the read operation as long as it is performed in a linear region. In order to verify the expectation, the same device is measured in the control sequence which is shown in Fig. 17. After writing both sets of data and holding them instantaneously, the WL is raised to 0.8 V and the BL is raised to 0.2 V to keep reading the data. We monitor the drain currents for both sets of data after the elapse of t_{RET} which is the data read duration. If, as is the case of the data hold, the dynamic transition effect of the BL and the WL can be considered as accumulation of static effect of each BL and WL amplitude, the worst case condition for the retention time is regarded to exist between the condition in Fig. 13 and that in Fig. 17, because these two are the situations where charging to the body and discharging from it occur most seriously in the two extreme cases. Fig. 18 is the result of I_0 and I_1 versus t_{RET}. Not only I_0 but also I_1 degrades as t_{RET} increases. This reason can be understood if we look at the device simulation results in Fig. 7. The potential of the data "1" cell's body is coupled up to a positive level with respect to the source potential during the data "1" read. So, if this state is maintained for a long time, the holes gradually flow out of the body to the source because the pn junction is forward-biased, albeit less than V_f. This makes the threshold voltage of the "1" cell transistor become the larger, leading to the smaller current. The degradation of the I_0, however, is milder than that in Fig. 14. This is explained by the fact

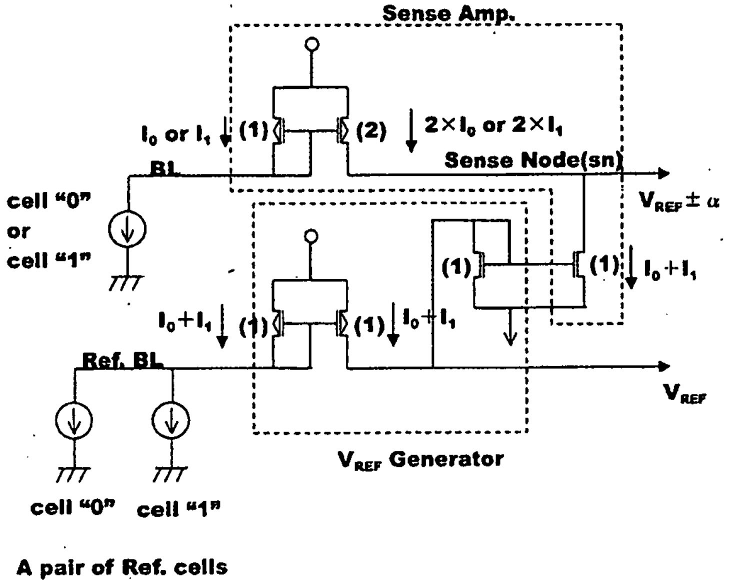


Fig. 19. The concept of the cell signal sensing system designed for the memory.

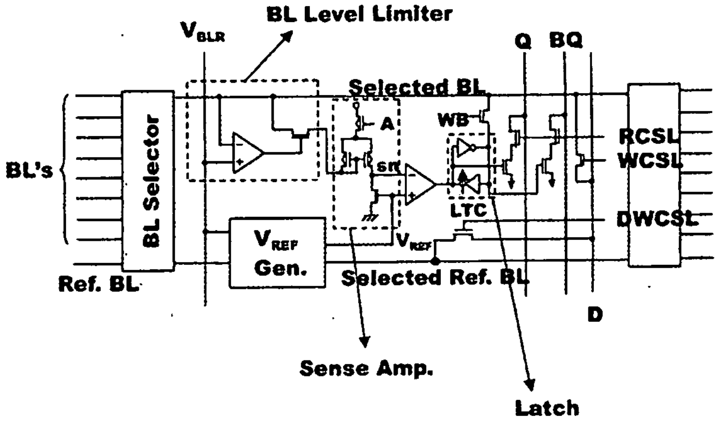


Fig. 20. The schematic view of the sense amp. circuit and other core circuits for the memory.

that the GIDL is smaller for the read condition than the hold one, because the gate voltage is positive during the read operation contrary to the negative for the hold state. So, overall, about 1 s of $t_{\rm RET}$ can be expected for the continuous read, being comparable to the $t_{\rm RET}$ for the hold condition.

V. MEMORY DESIGN USING THE FBC

We designed a 512-kb memory by using the FBC of size $7F^2$ ($F = 0.18$ μm). The key technology for designing an FBC memory is how the read signal can be sensed correctly as free as possible from the cell parameter variations in process and temperature. Fig. 19 describes the concept of the cell signal sensing system. A memory cell is connected to a BL, while a pair of reference cells, which are the same FBCs as the normal ones, are connected to a reference BL. One of the reference cells is written as data "1" and the other is written as data "0." The reference current, which is $I_0 + I_1$, is mirrored twice in the $V_{\rm REF}$ generator and the nFET which drives the sense node (sn) in the sense amp. circuit. On the other hand, the cell current, which is I_0 or I_1 depending on the cell data polarity, is doubled in the sense amp. circuit which loads the sn. So, two different currents are conflicting at the sn, making the voltage at the sn smaller than the $V_{\rm REF}$ for the "0" cell ($V_{\rm REF} - \alpha$) or larger than the $V_{\rm REF}$ for the "1" cell ($V_{\rm REF} + \alpha$). These voltage differences between $V_{\rm REF}$ and $V_{\rm REF} \pm \alpha$ can be amplified at the next stage circuit. The actual implementation of the sensing system is described in Fig. 20. Since the FBC is a nondestructive readout cell, one sense amp. circuit is designed per eight BLs which are supplied to a BL selector, and one of them is selected to be introduced to the sense amp. region. A reference BL is supplied to the $V_{\rm REF}$ generator which generates a reference voltage $V_{\rm REF}$

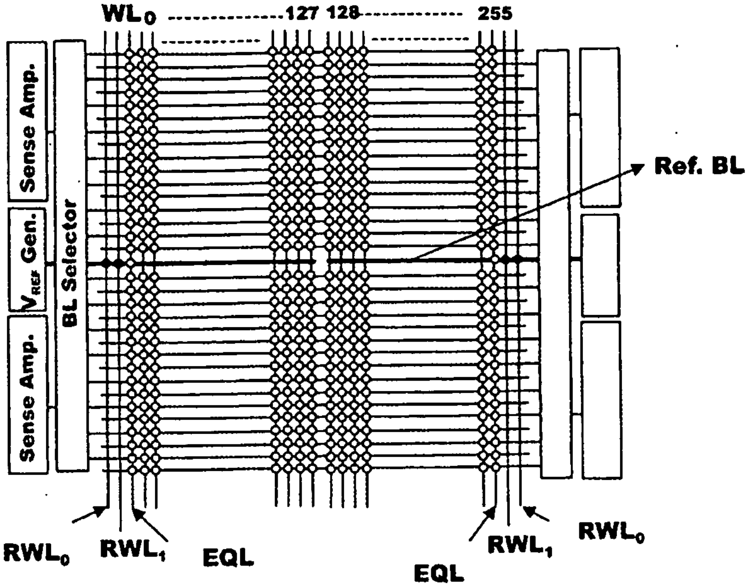


Fig. 21. The cell array architecture for the memory.

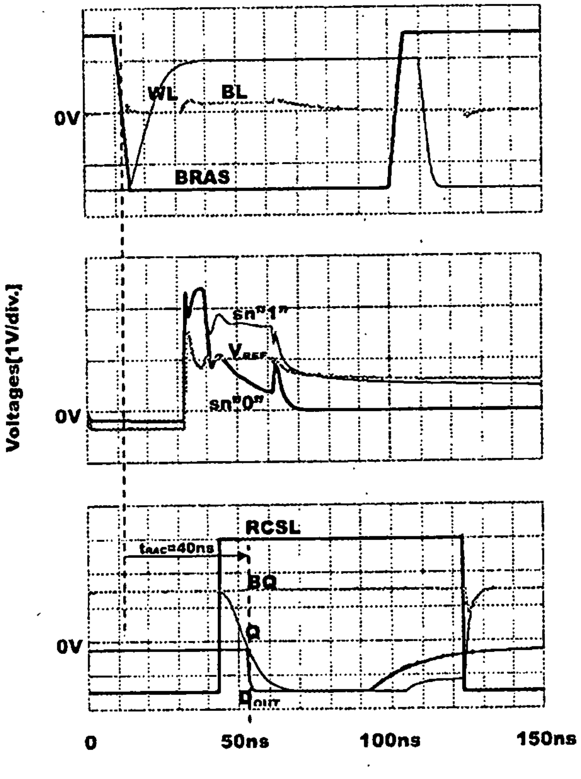


Fig. 22. The circuit simulation results of the memory.

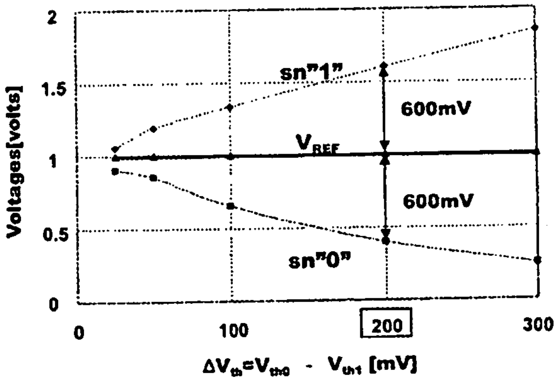


Fig. 23. The signals appearing on the sn and V_{REF}.

which is used in the sense amp. circuit. A differential amp and an nFET transfer gate forms a BL level limiter which limits the BL voltage at V_{BLR} during read which is set at 0.2 V. This limiter is necessary to keep the cell transistor from being biased at saturation during read, guaranteeing the nondestructive readout operation. The sensed data are amplified at a differential amp. circuit and are latched. The nFET gated by the write back signal (WB) is for a feedback loop which is used for refreshing. The nFETs gated by the read column select line (RCSL) are for reading the data to a pair of read lines Q and BQ and the nFET gated by the write column select line (WCSL) is for writing normal cells from a write data line D. The nFET gated by the dummy write column select line (DWCSL) is for writing data to reference cells. Fig. 21 is the cell array architecture of the memory and shows a unit of the sensing system consisting of 256 WLs, 32 BLs, and a reference BL which is divided into two parts. Each segment of the reference BL can be connected to a pair of reference cells by raising the reference word lines RWL_0 and RWL_1 and is supplied to the opposite side V_{REF} generators. The equalize signal (EQL) drives the gates of FBCs which equalize the BLs to GND

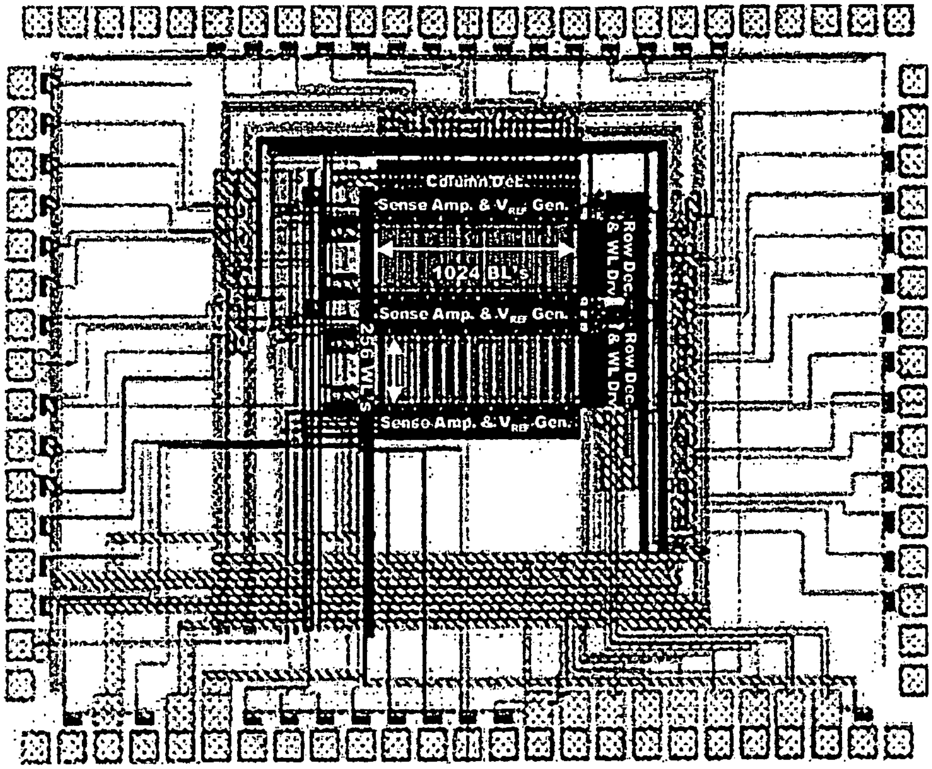

Column Dec.
Sense Amp. & V_{REF} Gen.
1024 BL's
Sense Amp. & V_{REF} Gen.
256 WL's
Sense Amp. & V_{REF} Gen.
Row Dec. & WL Drv.
Row Dec. & WL Drv.

Fig. 24. The mask image of the memory chip.

during precharge. The sensing system is double-ended and every other BLs is supplied to a sense amp. circuit through a BL selector. This sensing system compensates cell parameter variations ranging array to array, chip to chip, wafer to wafer, and lot to lot as common mode noises. A temperature variation of cell parameters is also compensated. The process variations within the 8-kb array within the sensing unit in Fig. 21(actual number of cells one pair of reference cells is responsible for is 4 kb) is of concern, proving that this sensing system is robust against the cell's process variations of long range space and of temperature.

Fig. 22 shows the results of circuit simulation for the 512-kb memory. This is a read operation performed by SPICE and a random access time is about 40 ns at 30 °C. Fig. 23 is the simulated signal which appears on the sn and V_{REF} with respect to the cell's threshold voltage difference between the "1" and the "0." For a 200-mV threshold voltage difference, ±600 mV will appear between the sn and V_{REF}, proving that this sensing system has a high sensitivity for the cell's data difference. The sense amp. circuit needs to be optimized, as we see that a 10-ns over-precharging time exists after the activation and that the phase of the negative feedback loop is not necessarily compensated enough, as is shown in the oscillation of the node sn in Fig. 22. We believe that an access time comparable with the conventional DRAMs one can be achieved if the circuit is optimized appropriately.

Fig. 24 is the mask data image of the 512-kb memory chip. There are two 256-kb arrays each includes 256 WLs and 1024 BLs. The cells were designed using a 0.18-μm minimum feature size and peripheral circuits and core circuits including the sense amp. were designed by using a 0.28-μm grand rule.

VI. CONCLUSION

Features of the FBC are summarized as follows.

A. Small Cell

Since the FBC consists of only an nFET on SOI, the cell size is small with an ability to be shrunk down to $4F^2$ by using self-aligned contact technologies.

B. Gain Cell

The FBC is a gain cell which can draw current from a BL. The signal amount itself is independent of a BL capacitance, making it possible for the BL to be longer than that of a conventional DRAM and contributing to increased cell efficiency. Though signal development time degrades as the BL becomes longer, this impact is rather mild. The length of the BL could be limited by the resistance of the total BL which becomes comparable to a cell transistor's channel resistance.

C. Nondestructive Readout Cell

The FBC is a nondestructive readout cell as far as it is read in a linear region. This feature is a must from a physical design point of view of a sense amplifier, because the FBC requires a relatively large area for the sense amp. (current sense) design and it is unrealistic to design it for every BL as the conventional DRAM sense amplifier circuit which is much more compact (dynamic voltage sense). This feature together with the previous one (gain cell) can make an FBC memory cell efficiency comparable or higher than the conventional DRAM one.

This sense amp. deign increases a busy rate for refreshing the FBC memory compared with the conventional DRAM's one unless the number of WLs which are activated simultaneously is increased from the conventional DRAM's number. Since this may increase the power of the FBC memory, we continue to pursue the design and layout of a sense amp circuit to be as compact as possible so as to decrease the number of BLs which are shared by a sense amp circuit.

D. Simple Process Cell

A process to make the FBC is simple and compatible with that of the Logic LSI, with a minor addition of steps to make pillars or without any addition if we choose a cell device parameter set shown in Fig. 12. The FBC is thus deemed to be embedded memory oriented.

E. Fast Cycle Time Cell

Since a large BL capacitance does not need to be restored during read cycle and the write buffer in the latch circuit in Fig. 20 can be designed sufficiently large enough to drive the BL fast during write, the cycle time of the FBC memory is expected faster than the conventional DRAM one after the circuit optimization is made as was stated in the previous section.

F. Scalable Cell

As is simulated in Section III, the drain current difference of the FBC between the data "1" and the data "0" is constant of the device feature size if the cell transistor is linearly shrunk in size and the body impurity concentration is heightened so as to keep the extent of the body bias effect constant. Therefore, the FBC memory can survive future miniaturization of transistors.

The retention time predicted in Section IV, 50 ms at 85 °C for $L = 0.18$ μm and $tSi = 1500$ Å is considered to be an average number among all cells in a chip. This number could be nearly doubled by using a thinner SOI of $t_{\text{Si}} = 750$ Å. It is not clear how large the standard deviation of the retention time is among them. However, even if it is improved from the conventional DRAM number by a simplified process to make the FBC, the average number of 100 ms is certainly insufficient to make the worst bit retention time larger than 100 ms, which is the specification of a stand-alone standard DRAM of a 100-Mb class chip. So, unless further improvement of the retention time, the FBC is only possible for some applications of embedded memories with relaxed specifications of the retention time. This situation is consistent with the FBC feature described in this section.

To improve the retention time and to make the FBC scalable with respect to the retention time is one of the biggest challenges we need to address. The retention time of a generation n is expressed as $t^{(n)}{}_{\text{RET}} = t^{(n-1)}{}_{\text{RET}}/\lambda$ where λ is a scaling factor by which the pn junction leak current per unit area increases by one generation. Therefore, we need to seek an FBC structure which realizes a constant pn junction leak current per unit area through generations.

In summary, we have proposed a concept of a new volatile RAM cell which consists of a MOSFET with its body floating and a 512-kb memory has been designed using a cell of the concept which is an nFET on SOI of the size $7F^2(= 0.18$ μm), though it has a potential to be further shrunk to $4F^2$ if self-aligned contacts are used. It needs to be refreshed but does not require any new material nor new structure. This cell has been proved to be scalable with respect to a signal and have a simple wafer process compatible with that of Logic LSI, making it a candidate for cells of future embedded memories. The retention time has also been predicted to be compatible with specifications of some embedded memories.

A cell signal sensing system has been designed which consists of a pair of reference cells which are written with both data and a current comparison circuit which compares the combined current of the two reference cells with the doubled current of a cell. This system is designed in a localized area so that process parameter variations of longer range than the system spread and temperature variation can be compensated as common mode noise. The predicted random access time is 40 ns. The cell efficiency is improved because this cell has a gain and is a nondestructive readout cell. The chip is in fabrication now and the measurement results of the memory are to be reported in another chance.

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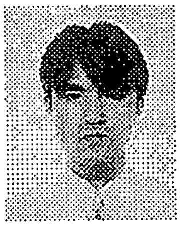

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Kazumasa Sunouchi, photograph and biography not available at the time of publication.

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Memory design using a one-transistor gain cell on SOI

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Abstract:
A 512-kb memory has been developed featuring a one-transistor gain cell of size 7F/sup 2/ (F = 0.18 /spl mu/m) on SOI. The cell named the floating body transistor cell (FBC) has the ability to achieve a 4F/sup 2/ cell using self-aligned contact technologies and is proved to be scalable with respect to a cell signal. A basic operation was verified by device simulation and hardware measurement. An array driving method is disclosed which makes selective write possible. A cell signal sensing system consisting of a pair of reference cells written opposite data and comparing the combined current with the doubled cell current is shown to be robust against cell parameter variations in process and temperature. A random access time of 40 ns was simulated. Nondestructive readout and C/sub b//C/sub s/. free signal development drastically improve cell efficiency.

Index Terms:
DRAM chips integrated circuit design nondestructive readout silicon-on-insulator 0.18 micron 40 ns 4F/sup 2/ cell 512 kbit DRAM cell SOI Si array driving method cell signal sensing system floating body transistor cell memory design nondestructive readout one-transistor gain cell reference cells selective write self-aligned contact technologies

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Documents that cite this document
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